AN3001
Application note

Demonstration board user guidelines for the TS4657 single supply stereo digital audio line driver

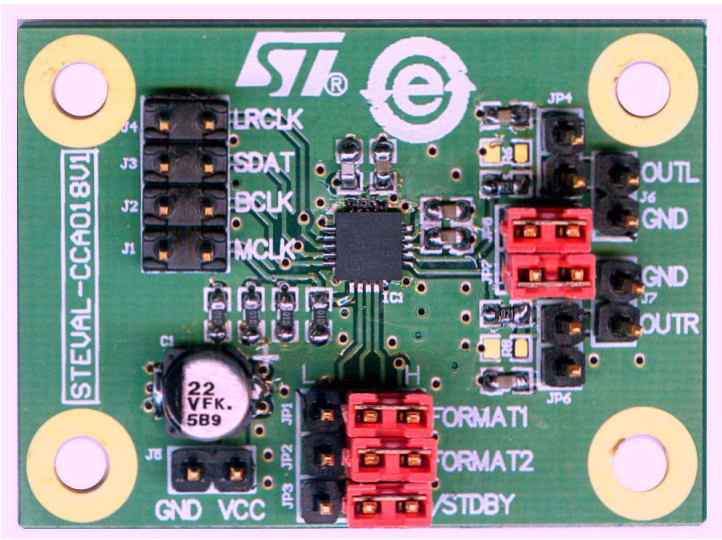
Introduction

This application note focuses on the TS4657 demonstration board, designed to evaluate STMicroelectronics' TS4657 device.

This document provides:

- a brief description of the TS4657 device.
- a description of the demonstration board and all of its components.
- the layout of the demonstration board.

Figure 1. TS4657 demonstration board



1 About the TS4657

The TS4657 is a stereo digital-to analog-converter (DAC) that integrates a high-performance audio line driver capable of generating a 2.2 Vrms output level from a single 3.0 to 5.5 V supply.

One single supply is sufficient for the digital and analog parts of the circuit, thus eliminating the need for external regulators.

The TS4657 is a low-power consumption device. It features only 22 mW power dissipation at a 3.0 V power supply in full operation.

A 16-bit multi-bit sigma delta DAC is used, operating at 256xFs with oversampling digital interpolation filters. The digital audio data can be 16- to 24-bit long and sample rates from 32 to 48 kHz are supported.

The output stage signal is ground-referenced by using an internal self-generated negative power supply, and as such external bulky output coupling capacitors are not necessary.

The TS4657 features the following.

- Power supply range: 3.0 V to 5.5 V.
- Audio line output: 2.2 Vrms for all V_{CC} range.
- 16- to 24-bit audio data format stereo DAC, 32 to 48 kHz sample rate.
- I²S, right- or left-justified compatible digital audio interface.
- 95 dB SNR A-weighted at 48 kHz, V_{CC} = 5 V.
- Low current consumption of 7.4 mA at V_{CC} = 3.0 V, full operation.
- Internal negative power supply to ensure ground-referenced, capless outputs.
- No necessity for an external capacitor for negative power supply generation.
- Integrated structure to suppress pop and click noise
- Standby mode active low.
- QFN20 package, 4 mm x 4 mm,500 µm pitch.

Refer to the datasheet entitled "*Single supply stereo digital audio line driver with 2.2 Vrms capless outputs*" for complete information on the TS4657.

2 Description of the demonstration board

The TS4657 demonstration board has been designed for evaluation purposes. The TS4657 device is soldered on a two-layer PCB.

Some key features of the TS4657 can be directly controlled through connectors or jumpers on the demonstration board (*Table 1*).

Table 1. Demonstration board connectors

Connector	Description
J1	MCLK: master clock input
J2	BCLK: bit clock input
J3	SDAT: serial data input
J4	LRCLK: left right clock input (channel selector input)
J5	Power supply connector (V_{CC} and GND). Power supply voltage of the TS4657 from 3.0 to 5.5 V.
J6	Left audio output
J7	Right audio output
JP1	Allows selection of level on Format1 pin. Format1 and Format2 pins select the digital input format (see *section 4.1.2 Digital audio input format* in the TS4657 datasheet). If the jumper is removed, it is possible to control the Format1 by an external logic signal (see *section 3.3 DAC and output stage performances* in the TS4657 datasheet).
JP2	Allows selection of level on Format2 pin. Format1 and Format2 pins select the digital input format (see *section 4.1.2 Digital audio input format* in the TS4657 datasheet). If the jumper is removed, it is possible to control the Format2 by an external logic signal (see *section 3.3 DAC and output stage performances* in the TS4657 datasheet).
JP3	Controls the chip standby (JP1:1-2 = circuit activated, 2-3 = circuit in standby mode). If the jumper is removed, it is possible to control the standby by an external logic signal (see *section 3.3 DAC and output stage performances* in the TS4657 datasheet).
JP4	Allows connection of the C6 capacitor (used for the left output filter; see *Section 3.3: Output filters on page 6*).
JP5	Allows short-circuiting of the R5 resistor (used for the left output filter; see *Section 3.3: Output filters on page 6*).
JP6	Allows connection of the C7 capacitor (used for the right output filter; see *Section 3.3: Output filters on page 6*).
JP7	Allows short-circuiting of the R7 resistor (used for the right output filter; see *Section 3.3: Output filters on page 6*).

Caution: When you apply the power supply through J5, do not invert the polarity as doing so will damage the chip.

Figure 2. Schematic diagram

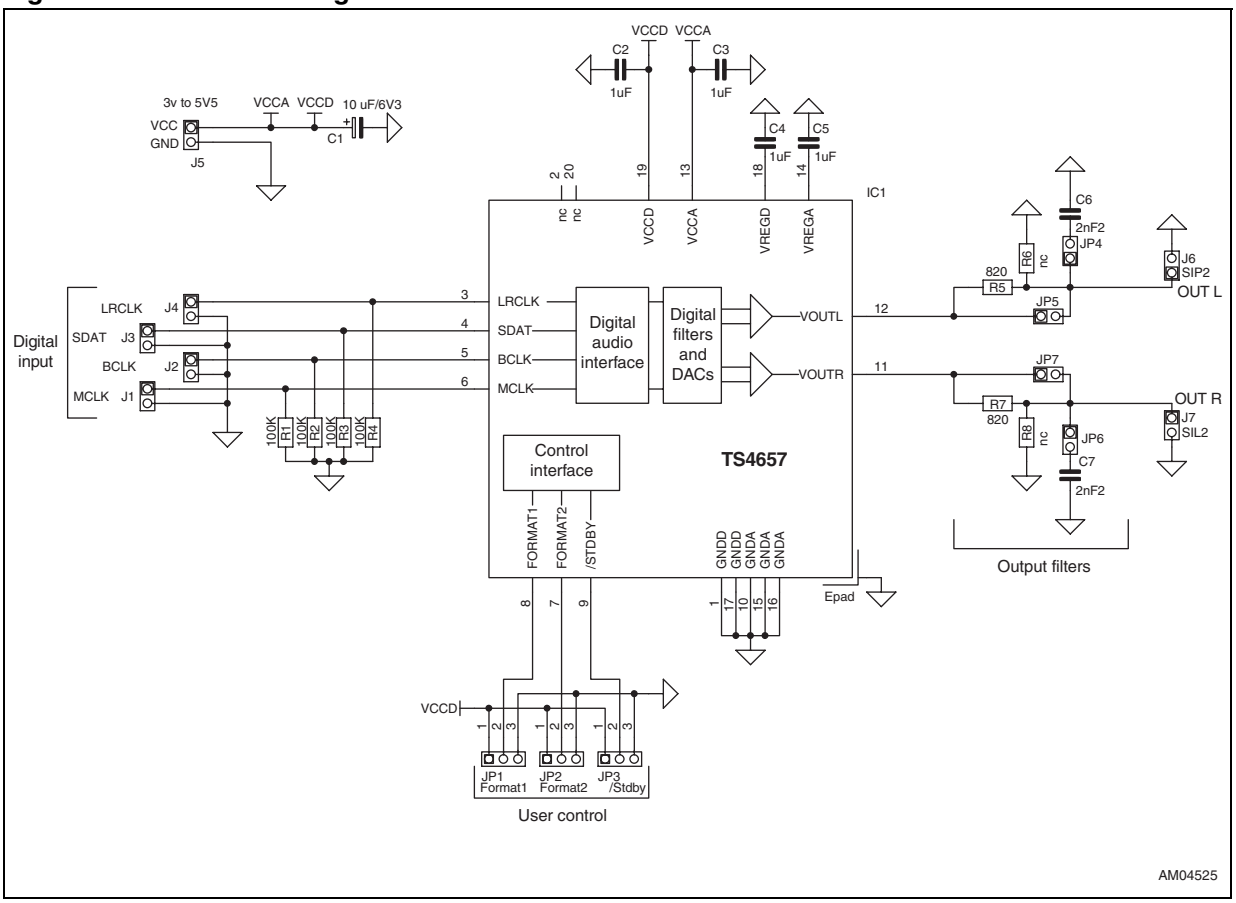


Table 2. Component list for the demonstration board

Name	Quantity	Description
C1	1	10 µF/6.3 V +/-20 %, SMD electrochemical capacitor
C2, C3, C4, C5	4	1 µF/10 V X5R, +/-10 %, SMD ceramic capacitors 0603
C6,C7	2	2.2 nF/50 V X7R, +/-10 %, SMD ceramic capacitors 0603
R1, R2, R3, R4	4	100 K/1 %, 0.063 W, SMD resistors, 0603
R5, R7	2	820 ohms/1 %, 0.063 W, SMD resistors, 0603
R6, R8	2	Not connected (see *Section 3.4: Optional measurement loads on page 7*)
J1, J2, J3, J4, J5, J6, J7, JP4, JP5, JP6, JP7	11	2-pin header 2.54 mm pitch
JP1, JP2, JP3	3	3-pin header 2.54 mm pitch
IC1	1	TS4657IQT

3 Configuring the demonstration board

3.1 Serial data input configuration

The TS4657 receives serial digital audio data through a 3-wire interface. SDAT is the serial audio data input. The data is entered MSB first and is a two's complement. The data can be I^2S, right- or left-justified. The data format is chosen with the control pins FORMAT1 and FORMAT2 as detailed in *Table 3*.

The level on both of these pins should be fixed before waking-up the chip.

Table 3. Digital audio data formats supported by the TS4657

FORMAT2	FORMAT1	Data Format	BCLK/LRCLK ratio	
			Min	Max
0	0	Right-justified, 16-bit data Data valid on rising edge of BCLK	32	256
0	1	Right-justified, 24-bit data Data valid on rising edge of BCLK	48	256
1	0	Left-Justified, 16-bit up to 24-bit data Data valid on rising edge of BCLK	2 x number of bits of data	256
1	1	I²S, 16-bit up to 24-bit data Data valid on rising edge of BCLK	2 x number of bits of data	256

3.2 Sample rate capability

Three external clock signals are applied to the TS4657. The MCLK is the external master clock applied by the audio data processor. The LRCLK is the channel frequency, also called LEFT/RIGHT clock, at which the digital words for each channel are input to the device. The LRCLK clock is the sample rate of the audio data. The ratio MCLK/LRCLK must be an integer, as shown in *Table 4*.

The BCLK is the bit clock and represents the clock at which the audio data is serially shifted into the audio port. BCLK is linked to LRCLK. The minimum required BCLK frequency is twice the audio sample rate multiplied by the number of bits in each audio word. Refer to *Table 3* for the BCLK/LRCLK ratio. MCLK, LRCLK and BCLK must be synchronous clock signals.

Table 4. Audio data sampling rates

LRCLK (kHz)	MCLK (MHz)
	256x
32	8.192
44.1	11.2896
48	12.288

3.3 Output filters

The output filter embedded on the demonstration board is a low-pass filter made up of a resistor and a capacitor. In this configuration, the -3 dB cut-off frequency in Hz is:

$$\frac{1}{2\pi \times R \times C}$$

with $R = R_5 = R_7$ in ohms, C in farads and $C = C_6 = C_7$.

Figure 3 and *Figure 4* show the jumper settings to use depending on whether or not the output filters are necessary. If the output filters are not necessary, JP5 and JP7 are shorted and JP4 and JP6 are opened. If the output filters are required, JP4 and JP6 are shorted and JP5 and JP7 are opened.

Figure 3. Output stage without output filters

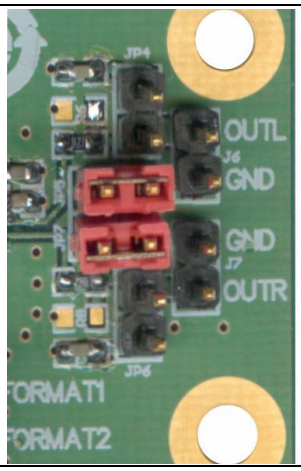
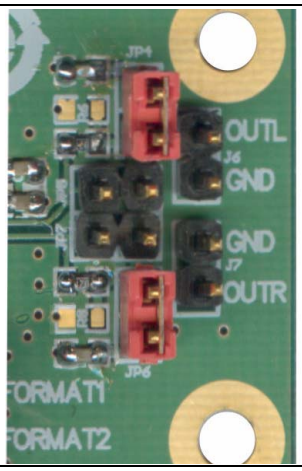


Figure 4. Output stage with output filters



3.4 Optional measurement loads

As shown in *Figure 2 on page 4*, there are two resistors (R6 and R8) that are not connected on the demonstration board. These resistors are used to measure the performances of the TS4657 with different loads. After the test, it is best to remove them and load the TS4657 with the application only.

The load on both outputs should be higher or equal to 5 k. Generally, the standard load for the audio line is 10 k (10 K/1 %, 0.063 W, SMD resistors, 0603).

3.5 Specific considerations

The TS4657 utilizes a power management unit to supply its internal structures.

A self-generated negative supply allows the drivers to be powered from positive and negative supplies, thus increasing the output signal amplitude. This internal negative supply switches at a higher frequency than traditional architectures, derived from the master clock MCLK. This structure uses an original design that allows suppressing the flying or floating capacitors. Therefore, only four small 1 µF decoupling capacitors are necessary for VCCA/VCCD and VREGA/VREGD.

Furthermore, the self-generated negative supply allows the amplifier outputs to be centered around zero, thus the bulky output coupling capacitors can be removed.

As mentioned previously, the MCLK is used internally to supply some blocks. It is therefore not recommended to switch off the MCLK during normal operation.

To properly power-down the device, MCLK, BCLK and LRCLK should be switched off after the STDBY signal.

The power-down time is very short and can be considered as zero.

4 Demonstration board layout

The following figures show the layers and top and bottom views of the demonstration board.

Figure 5. PCB top overlay

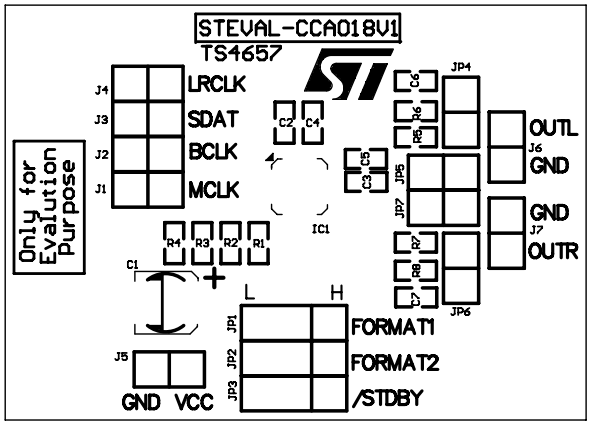


Figure 6. PCB top layer

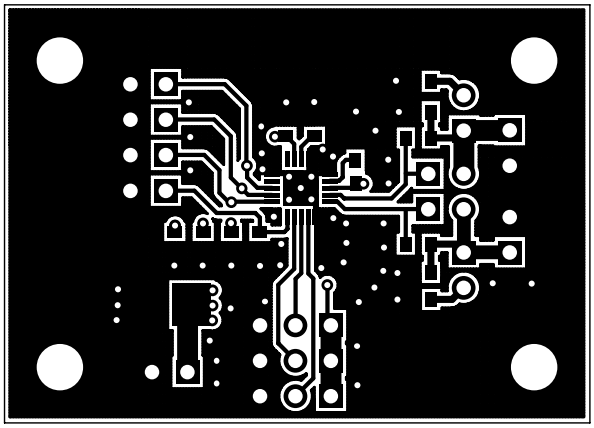


Figure 7. PCB bottom overlay

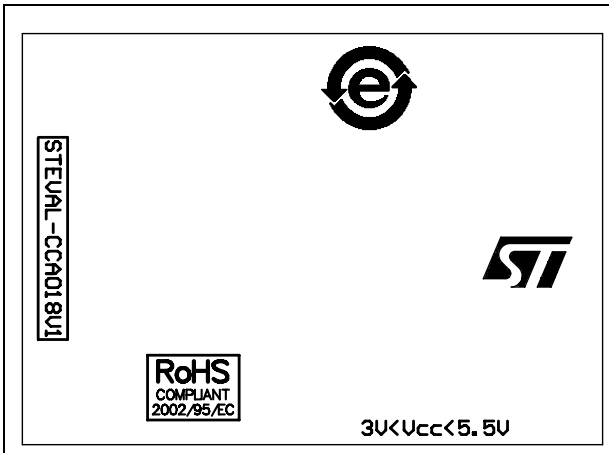


Figure 8. PCB bottom layer

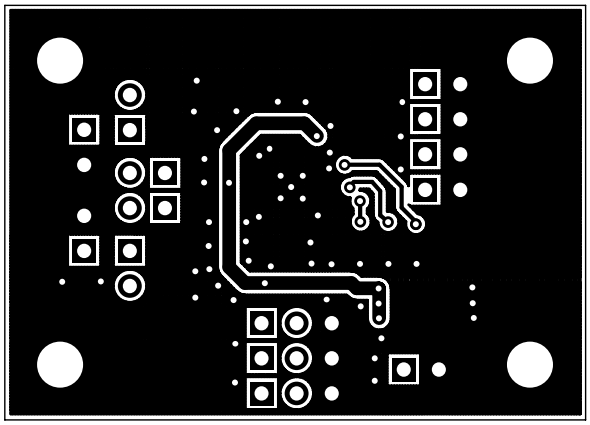


Figure 9. Top view of the demonstration board

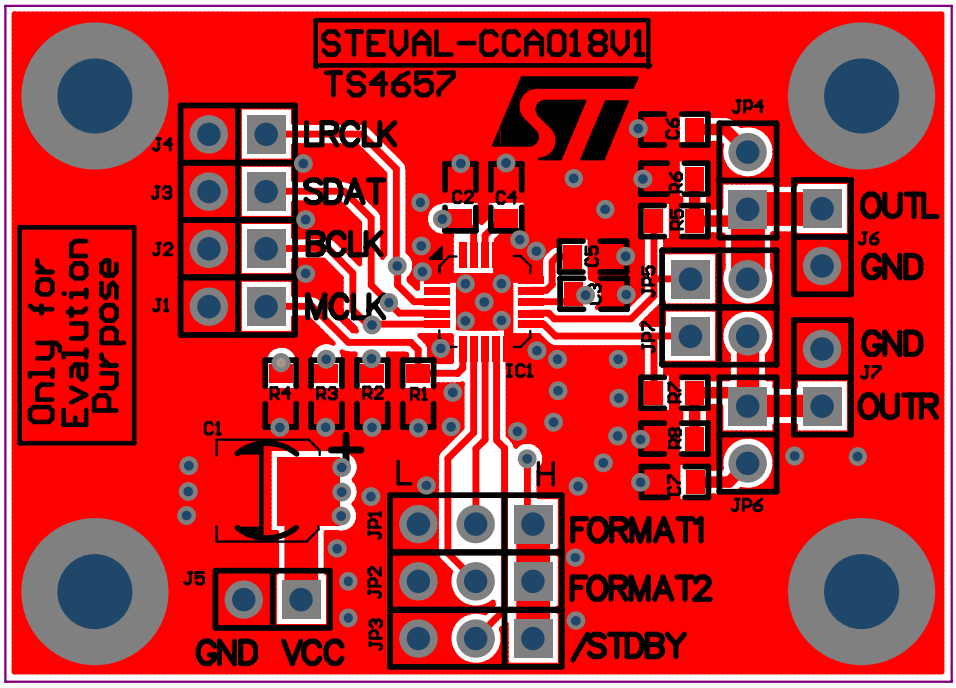
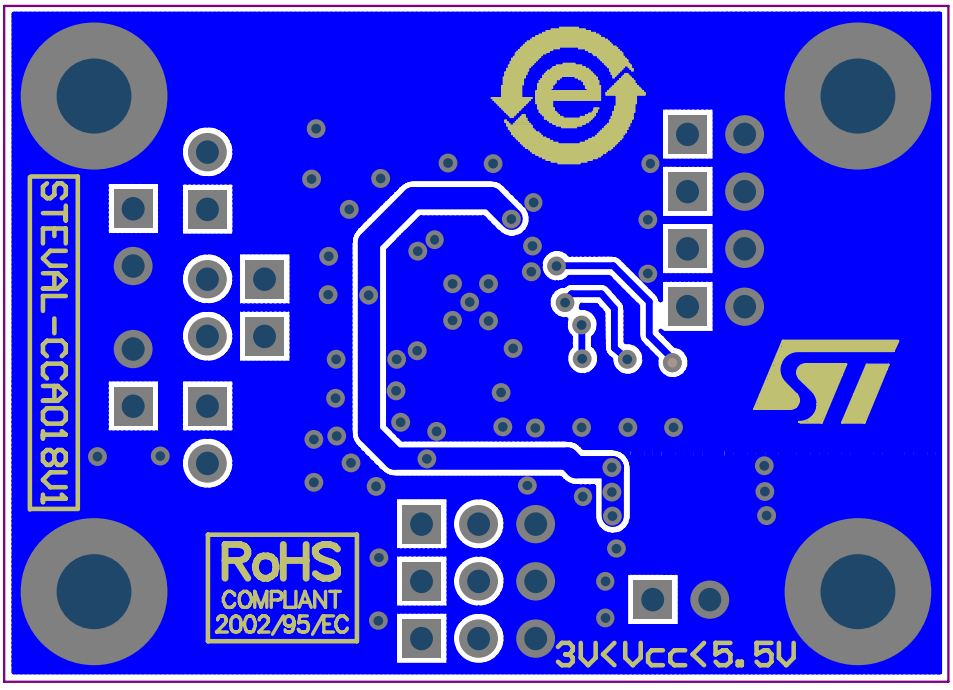


Figure 10. Bottom view of the demonstration board



5 Conclusion

To order the board online, go to *http://www.st.com/stonline/domains/buy/buy_dev.htm*, and use the order code STEVAL-CCA018V1.

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
03-Jul-2009	1	Initial release.