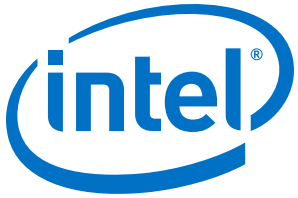

Stratix 10 Device Datasheet

S10-DATASHEET
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Contents

1 Stratix® 10 Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Stratix® 10 devices.

Table 1. Stratix 10 Device Grades and Speed Grades Supported

Device Grade	Speed Grade Supported
Extended	• –E1V (fastest) • –E2V • –E2L • –E3V • –E3X
Industrial	• –I1V • –I2V • –I2L • –I3V • –I3X

The suffix after the speed grade denotes the power options offered in Stratix 10 devices.

- V—SmartVID with standard static power
- L—0.85 V fixed voltage with low static power
- X—0.80 V fixed voltage with lowest static power

1.1 Electrical Characteristics

The following sections describe the operating conditions and power consumption of Stratix 10 devices.

1.1.1 Operating Conditions

Stratix 10 devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Stratix 10 devices, you must consider the operating requirements described in this section.

The Maximum Allowed Overshoot During Transitions specifications will be available in a future release of the *Stratix 10 Device Datasheet*.

1.1.1.1 Absolute Maximum Ratings

This section defines the maximum operating conditions for Stratix 10 devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2. Absolute Maximum Ratings for Stratix 10 Devices—Preliminary

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CC}	Core voltage power supply	—	–0.50	1.26	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	—	–0.50	1.26	V
V_{CCERAM}	Embedded memory power supply	—	–0.50	1.24	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	–0.50	2.46	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	—	–0.50	2.46	V
V_{CCIO_SDM}	Configuration pins power supply	—	–0.50	2.46	V
V_{CCIO}	I/O buffers power supply	3 V I/O	–0.50	4.10	V
		LVDS I/O [1]	–0.50	2.46	V
V_{CCA_PLL}	Phase-locked loop (PLL) analog power supply	—	–0.50	2.46	V
V_{CCT_GXB}	Transmitter analog power supply	—	–0.50	1.47	V

continued...

1 The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

Symbol	Description	Condition	Minimum	Maximum	Unit
V_{CCR_GXB}	Receiver analog power supply	—	–0.50	1.47	V
V_{CCH_GXB}	Transmitter output buffer power supply	—	–0.50	2.46	V
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	—	–0.50	1.30	V
V_{CCIO_HPS}	HPS I/O buffers power supply	LVDS I/O [1]	–0.50	2.46	V
V_{CCPLL_HPS}	HPS PLL power supply	—	–0.50	2.46	V
I_{OUT}	DC output current per pin	—	–25	40	mA
T_J	Operating junction temperature	—	–55	125	°C
T_{STG}	Storage temperature (no bias)	—	–65	150	°C

1.1.1.2 Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Stratix 10 devices.

1.1.1.2.1 Recommended Operating Conditions

Table 3. Recommended Operating Conditions for Stratix 10 Devices—Preliminary

This table lists the steady-state voltage values expected for Stratix 10 devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum [2]	Typical	Maximum [2]	Unit
V_{CC}	Core voltage power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V	0.77	—	0.97	V
		–E2L, –I2L	0.82	0.85	0.88	V
		–E3X, –I3X	0.77	0.8	0.83	V
V_{CCP}	Periphery circuitry and transceiver fabric interface power supply	–E1V, –I1V, –E2V, –I2V, –E3V, –I3V	0.77 – 0.91	0.8 – 0.94	0.83 – 0.97	V
		–E2L, –I2L	0.82	0.85	0.88	V

continued...

2 This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the power distribution network (PDN) tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Condition	Minimum [2]	Typical	Maximum [2]	Unit
		–E3X, –I3X	0.77	0.8	0.83	V
V_{CCIO_SDM}	Configuration pins power supply	1.8 V	1.71	1.8	1.89	V
$V_{CCPLLDIG\_SDM}$	Secure Device Manager (SDM) block PLL digital power supply	—	0.87	0.9	0.93	V
V_{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
$V_{CCPFUSE\_SDM}$	Fuse block writing power supply	—	2.35	2.4	2.45	V
V_{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V_{CCERAM}	Embedded memory power supply	0.9 V	0.87	0.9	0.93	V
V_{CCBAT} [3]	Battery back-up power supply (For design security volatile key register)	1.8 V	1.71	1.8	1.89	V
		1.2 V	1.14	1.2	1.26	V
V_{CCPT}	Power supply for programmable power technology and I/O pre-driver	1.8 V	1.71	1.8	1.89	V
V_{CCIO}	I/O buffers power supply	3.0 V (for 3 V I/O only)	2.85	3	3.15	V
		1.8 V	1.71	1.8	1.89	V
		1.5 V	1.425	1.5	1.575	V
		1.2 V	1.14	1.2	1.26	V
V_{CCIO_UIB}	Power supply of the I/O in the universal interface bus region	1.2 V	0.9	1.2	1.5	V
V_{CCA_PLL}	PLL analog voltage regulator power supply	—	1.71	1.8	1.89	V
V_{REFP_ADC}	Precision voltage reference for voltage sensor	—	1.2475	1.25	1.2525	V
V_I [4]	DC input voltage	3 V I/O	–0.3	—	3.6	V

continued...

2 This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the power distribution network (PDN) tool for the additional budget for the dynamic tolerance requirements.

3 If you do not use the design security feature in Stratix 10 devices, connect V_{CCBAT} to a 1.8 V power supply. Stratix 10 power-on reset (POR) circuitry monitors V_{CCBAT}.

Symbol	Description	Condition	Minimum [2]	Typical	Maximum [2]	Unit
		LVDS I/O	–0.3	—	2.46	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	–40	—	100	°C
t_{RAMP} [56]	Power supply ramp time	Standard POR	200 µs	—	100 ms	—

Table 4. Temperature Compensation for SmartVID for Stratix 10 Devices—Preliminary

The Secure Device Manager (SDM) can detect the device temperature and adjust the voltage by communicating with an external power management system. Adjustment is made by the SDM after the sensor detects temperature setting is below 10 °C or above 20 °C from the targeted temperature.

Temperature Threshold	SmartVID Voltage Adjustment (After 30 ms)
< 10 °C	30 mV
> 20 °C	–30 mV

2 This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the power distribution network (PDN) tool for the additional budget for the dynamic tolerance requirements.

4 The LVDS I/O values are applicable to all dedicated and dual-function configuration I/Os.

5 This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

6 t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.

1.1.1.2.2 Transceiver Power Supply Operating Conditions

Table 5. Transceiver Power Supply Operating Conditions for Stratix 10 GX/SX L- and H-Tile Devices—Preliminary

Symbol	Description	Condition [7]	Minimum [8]	Typical	Maximum	Unit
$V_{CCT\_GXB[L,R]}$	Transmitter power supply	Chip-to-Chip [9] ≤ 17.4 Gbps Or Backplane [10] ≤ 12.5 Gbps	1.0	1.03	1.06	V
$V_{CCR\_GXB[L,R]}$	Receiver power supply	Chip-to-Chip [9] ≤ 17.4 Gbps Or Backplane [10] ≤ 12.5 Gbps	1.0	1.03	1.06	V
$V_{CCH\_GXB[L,R]}$	Transceiver high voltage power	—	1.710	1.8	1.890	V

Table 6. Transceiver Power Supply Operating Conditions for Stratix 10 GX/SX/TX/MX E-Tile Devices—Preliminary

Symbol	Description	Minimum [11]	Typical	Maximum [11]	Unit
V_{CCERT}	Transceiver power supply	0.87	0.9	0.93	V
V_{CCERT_PLL}	Transceiver PLL power supply	0.87	0.9	0.93	V
V_{CCEHT}	Analog power supply [11]	1.067	1.1	1.133	V

continued...

7 These data rate ranges vary depending on the transceiver speed grade. Refer to Transceiver Performance for Stratix 10 GX/SX Devices for exact data rate ranges.

8 This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

9 Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ± 20 mV.

10 Backplane applications assume advanced equalization circuitry, such as decision feedback equalization (DFE), is enabled to compensate for signal impairments. Chip-to-chip links are assumed to be applications with short reach channels that do not require DFE.

11 This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Symbol	Description	Minimum [11]	Typical	Maximum [11]	Unit
V_{CCL}	Periphery circuitry power supply	0.725	0.75	0.775	V
$V_{CCN2P5V\_IO}$	LVPECL REFCLK power supply	2.375	2.5	2.625	V
V_{CCR}	Transceiver high voltage power supply	1.71	1.8	1.89	V

Note: Most VCCR_GXB and VCCT_GXB pins associated with unused transceiver channels can be grounded on a per-side basis to minimize power consumption. Refer to the *Stratix 10 GX, GT, and SX Device Family Pin Connection Guidelines* and the Quartus® Prime pin report for information about pinning out the package to minimize power consumption for your specific design.

Related Links

Stratix 10 GX, GT, and SX Device Family Pin Connection Guidelines

1.1.1.2.3 HPS Power Supply Operating Conditions

Table 7. HPS Power Supply Operating Conditions for Stratix 10 Devices—Preliminary

This table lists the steady-state voltage and current values expected for Stratix 10 system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Stratix 10 Devices table for the steady-state voltage values expected from the FPGA portion of the Stratix 10 SoC devices.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCL_HPS}	HPS core voltage and periphery circuitry power supply	HPS voltage	0.90	0.95	1.00	V
		SmartVID	0.76 – 0.84	0.8 – 0.94	0.84 – 0.987	V
$V_{CCPLLDIG\_HPS}$	HPS PLL digital power supply	HPS voltage	0.90	0.95	1.00	V
		SmartVID	0.76 – 0.84	0.8 – 0.94	0.84 – 0.987	V
V_{CCPLL_HPS}	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V_{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

11 This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

1.1.1.3 DC Characteristics

The pin capacitance specifications will be available in a future release of the *Stratix 10 Device Datasheet*.

1.1.1.3.1 Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus Prime PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.

The Quartus Prime PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

1.1.1.3.2 I/O Pin Leakage Current

Table 8. I/O Pin Leakage Current for Stratix 10 Devices—Preliminary

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–80	80	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–80	80	µA

1.1.1.3.3 Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 9. Bus Hold Parameters for Stratix 10 Devices—Preliminary

Parameter	Symbol	Condition	V_{CCIO} (V)								Unit
			1.2		1.5		1.8		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max)	8	—	12	—	30	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min)	–8	—	–12	—	–30	—	–70	—	µA

continued...

Parameter	Symbol	Condition	V_{CCIO} (V)								Unit
			1.2		1.5		1.8		3.0		
			Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, overdrive current	I_{ODL}	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.38	1.13	0.68	1.07	0.8	2	V

1.1.1.3.4 OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 10. OCT Calibration Accuracy Specifications for Stratix 10 Devices—Preliminary

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
48-Ω, 60-Ω, 80-Ω, and 240-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
25-Ω and 50-Ω R_S	Internal series termination with calibration (25-Ω and 50-Ω setting)	V_{CCIO} = 3.0, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 40-Ω, 48-Ω, 60-Ω, 80-Ω, 120-Ω, and 240-Ω setting)	POD12 I/O standard, V_{CCIO} = 1.2	±15	±15	±15	%
34-Ω, 48-Ω, 80-Ω, and 240-Ω R_T	Internal parallel termination with calibration (34-Ω, 48-Ω, 80-Ω, and 240-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%

continued...

Symbol	Description	Condition (V)	Calibration Accuracy			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
40-Ω, 60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω R_T	Internal parallel termination with calibration (25-Ω setting)	V_{CCIO} = 1.5	–10 to +40	–10 to +40	–10 to +40	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%

1.1.1.3.5 OCT Without Calibration Resistance Tolerance Specifications

Table 11. OCT Without Calibration Resistance Tolerance Specifications for Stratix 10 Devices—Preliminary

This table lists the Stratix 10 OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance			Unit
			–E1, –I1	–E2, –I2	–E3, –I3	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8, 1.5	TBD	TBD	TBD	%
		V_{CCIO} = 1.2	TBD	TBD	TBD	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8, 1.5	TBD	TBD	TBD	%
		V_{CCIO} = 1.2	TBD	TBD	TBD	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 1.8	±25	±35	±40	%

Figure 1. Equation for OCT Variation Without Recalibration—Preliminary

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

1.1.1.3.6 Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.

Table 12. Internal Weak Pull-Up Resistor Values for Stratix 10 Devices—Preliminary

Symbol	Description	Condition (V)	Nominal Value	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Related Links

Stratix 10 Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

1.1.1.4 I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix 10 devices.

For minimum voltage values, use the minimum V_{CCIO} values. For maximum voltage values, use the maximum V_{CCIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Links

Recommended Operating Conditions on page 5

1.1.1.4.1 Single-Ended I/O Standards Specifications

Table 13. Single-Ended I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{IL}(V)		V_{IH}(V)		V_{OL} (V)	V_{OH} (V)	I_{OL} [12] (mA)	I_{OH} [12] (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
1.8 V	1.71	1.8	1.89	-0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 × V_{CCIO}	0.65 × V_{CCIO}	V_{CCIO} + 0.3	0.25 × V_{CCIO}	0.75 × V_{CCIO}	2	–2

1.1.1.4.2 Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 14. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.45	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.31	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}

continued...

12 To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.0-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	$V_{CCIO}/2$	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	$V_{CCIO}/2$	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 × V_{CCIO}	0.5 × V_{CCIO}	0.53 × V_{CCIO}	—	$V_{CCIO}/2$	—
HSUL-12	1.14	1.2	1.3	0.49 × V_{CCIO}	0.5 × V_{CCIO}	0.51 × V_{CCIO}	—	—	—
POD12	1.16	1.2	1.24	—	Internally calibrated	—	—	V_{CCIO}	—

1.1.1.4.3 Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 15. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix 10 Devices—Preliminary

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} [13] (mA)	I_{OH} [13] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 × V_{CCIO}	0.8 × V_{CCIO}	16	–16
SSTL-135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
SSTL-125	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 × V_{CCIO}	0.8 × V_{CCIO}	—	—
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8

continued...

13 To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{OL} [13] (mA)	I_{OH} [13] (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 × V_{CCIO}	0.75 × V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 × V_{CCIO}	0.9 × V_{CCIO}	—	—
POD12	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	(0.7 – 0.15) × V_{CCIO}	(0.7 + 0.15) × V_{CCIO}	—	—

1.1.1.4.4 Differential SSTL I/O Standards Specifications

Table 16. Differential SSTL I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{SWING(AC)}$ (V)		$V_{X(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Max	Min	Max
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	0.5	V_{CCIO} + 0.6	$V_{CCIO}/2$ – 0.175	$V_{CCIO}/2$ + 0.175
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	[14]	$2(V_{IH(AC)} – V_{REF})$	$2(V_{REF} – V_{IL(AC)})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$ + 0.15
SSTL-135	1.283	1.35	1.45	0.18	[14]	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$ + 0.15
SSTL-125	1.19	1.25	1.31	0.18	[14]	$2(V_{IH(AC)} – V_{REF})$	$2(V_{IL(AC)} – V_{REF})$	$V_{CCIO}/2$ – 0.15	$V_{CCIO}/2$ + 0.15

13 To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

14 The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

1.1.1.4.5 Differential HSTL and HSUL I/O Standards Specifications

Table 17. Differential HSTL and HSUL I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{DIF(AC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.4	—	0.78	—	1.12	0.78	—	1.12
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.4	—	0.68	—	0.9	0.68	—	0.9
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	0.3	V_{CCIO} + 0.48	—	0.5 × V_{CCIO}	—	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}
HSUL-12	1.14	1.2	1.3	$2(V_{IH(DC)} - V_{REF})$	$2(V_{REF} - V_{IH(DC)})$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{REF} - V_{IH(AC)})$	0.5 × V_{CCIO} − 0.12	0.5 × V_{CCIO}	0.5 × V_{CCIO} +0.12	0.4 × V_{CCIO}	0.5 × V_{CCIO}	0.6 × V_{CCIO}

1.1.1.4.6 Differential I/O Standards Specifications

Table 18. Differential I/O Standards Specifications for Stratix 10 Devices—Preliminary

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) [15]		$V_{ICM(DC)}$ (V)			V_{OD} (V) [16]			V_{OCM} (V) [16]		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS [17]	1.71	1.8	1.89	100	—	0.05	D_{MAX} ≤700 Mbps	1.65	0.247	—	0.6	1.125	1.25	1.375
						1	D_{MAX} >700 Mbps	1.6						
RSDS [18]	1.71	1.8	1.89	100	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4

continued...

15 The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

16 R_L range: $90 \leq R_L \leq 110\ \Omega$.

17 For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 700 Mbps and 0.05 V to 1.65 V for data rates below 700 Mbps.

I/O Standard	V_{CCIO} (V)			V_{ID} (mV) [15]		$V_{ICM(DC)}$ (V)			V_{OD} (V) [16]			V_{OCM} (V) [16]		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
Mini-LVDS [19]	1.71	1.8	1.89	200	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL [20]	1.71	1.8	1.89	300	—	0.6	D_{MAX} ≤700 Mbps	1.7	—	—	—	—	—	—
						1	D_{MAX} >700 Mbps	1.6						

1.2 Switching Characteristics

This section provides the performance characteristics of Stratix 10 core and periphery blocks.

1.2.1 L-Tile Transceiver Performance Specifications

1.2.1.1 Transceiver Performance for Stratix 10 GX/SX L-Tile Devices

Table 19. L-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Chip-to-Chip [21] [22]	1 Gbps to 17.4 Gbps [23]	1.0	1.03	1.06	V
Backplane [21] [24]	1 Gbps to 12.5 Gbps [23]	1.0	1.03	1.06	V

15 The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

16 R_L range: 90 ≤ R_L ≤ 110 Ω.

18 For optimized RSDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.4 V.

19 For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.4 V to 1.325 V.

20 For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

21 Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ± 20 mV.

Table 20. L-Tile ATX PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	8.7	GHz
	Minimum Frequency	500	MHz

Table 21. L-Tile Fractional PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

Table 22. L-Tile CMU PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2450	MHz

1.2.1.2 Transceiver Specifications for Stratix 10 GX/SX L-Tile Devices

Table 23. L-Tile Reference Clock Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			

continued...

22 Chip-to-chip refers to transceiver links that are short reach and dont require advanced equalization such as decision feedback equalization (DFE).

23 Stratix 10 transceivers can support data rates below 1 Gbps through over sampling.

24 Backplane applications refer to ones which require advanced equalization, such as DFE enabled, to compensate for channel loss.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		50 [25]	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} =1.03 V	—	1.03	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) [26]	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz

continued...

25 The f_{MIN} is 29 MHz when the fPLL is used as a core PLL.

26 To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
$T_{SSC-MAX-PERIOD-SLEW}$	Max SSC df/dt			0.75	

Table 24. L-Tile Transceiver Clock Network Maximum Data Rate Specifications—Preliminary

Clock Network	Maximum Performance [27]			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	16	12.5	N/A	2 banks up and 2 banks down	Gbps

Table 25. L-Tile Receiver Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin [28]	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin [28]	—	-0.4	—	—	V

continued...

27 The maximum data rate depends on speed grade.

28 The device cannot tolerate prolonged operation at this absolute maximum.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration [29]	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration [29]	V_{CCR_GXB} = 1.03 V [30]	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins [31]	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{ICM} (AC and DC coupled) non-PCIe channels	V_{CCR_GXB} = 1.03 V	—	700	—	mV
	V_{CCR_GXB} = 1.12 V	—	750	—	mV
V_{ICM} (AC and DC coupled) PCIe channels	V_{CCR_GXB} = 1.03 V	—	650	—	mV
	V_{CCR_GXB} = 1.12 V	—	650	—	mV
t_{LTR} [32]	—	—	—	1	ms
t_{LTD} [33]	—	4	—	—	µs

continued...

29 DC coupling specifications are pending silicon characterization.

30 Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} and V_{CCT_GXB} = 1.12 V ± 20 mV.

31 The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

32 t_{LTR} is the time required for the receiver CDR to lock to the input reference clock frequency after coming out of reset.

33 t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
t_{LTD_manual}[34]	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$[35]	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR PPM tolerance	PCIe-only	-300	—	300	PPM
	All other protocols	-1000	—	1000	PPM

Table 26. L-Tile Transmitter Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O [36]			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.03 V	—	515	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.03 V	—	515	—	mV
Rise time [37]	20% to 80%	20	—	130	ps
Fall time [37]	80% to 20%	20	—	130	ps
Intra-differential pair skew [38]	TX V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	ps

34 t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

35 $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

36 High Speed Differential I/O is the dedicated I/O standard for the transmitter in Stratix 10 transceivers.

37 The Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Table 27. L-Tile Typical Transmitter V_{OD} Settings—Preliminary

Symbol	V_{OD} Setting	V_{OD}/V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}/V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50
	15	0.47
	14	0.43
	13	0.40
	12	0.37

38 In QPI mode, if V_{CM} < 0.17 V, the input Vid must be greater than 100 mV. If V_{CM} > 0.17 V, the input Vid must be greater than 70 mV.

Table 28. L-Tile Transmitter Channel-to-channel Skew Specifications—Preliminary

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps

Table 29. Transceiver Clocks Specifications for Stratix 10 GX/SX L-Tile Devices—Preliminary

Clock	Value	Unit
`reconfig_clk`	≤ 125	MHz
`fixed_clk` for the RX detect circuit	250 ± 20%	MHz

For OSC_CLK_1 specifications, refer to the External Configuration Clock Source Requirements section.

Related Links

- External Configuration Clock Source Requirements on page 49
- PLLs and Clock Networks

1.2.2 H-Tile Transceiver Performance Specifications

1.2.2.1 Transceiver Performance for Stratix 10 GX/SX H-Tile Devices

Table 30. H-Tile Transmitter and Receiver Data Rate Performance, VCCR_GXB and VCCT_GXB Specifications—Preliminary

Channel	Symbol/Description	Transceiver Speed Grades			Minimum	Typical	Maximum	
		-1	-2	-3				Unit
GX [39] [40]	Chip-to-Chip	1 Gbps to 17.4 Gbps [41]	1 Gbps to 17.4 Gbps [41]	1 Gbps to 17.4 Gbps [41]	1.0	1.03	1.06	V
	Backplane	1 Gbps to 17.4 Gbps [41]	1 Gbps to 17.4 Gbps [41]	1 Gbps to 17.4 Gbps [41]	1.0	1.03	1.06	V
GXT [42]	Chip-to-Chip	1 Gbps to 28.3 Gbps [41]	1 Gbps to 26 Gbps [41]	1 Gbps to 17.4 Gbps [41]	1.10	1.12	1.14	V
	Backplane	1 Gbps to 28.3 Gbps [41]	1 Gbps to 26 Gbps [41]	1 Gbps to 17.4 Gbps [41]	1.10	1.12	1.14	V

Table 31. H-Tile ATX PLL Performance—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 1	Transceiver Speed Grade 2	Transceiver Speed Grade 3	Unit
Supported Output Frequency	Maximum Frequency	14.15	13	8.7	GHz
	Minimum Frequency	500			MHz

39 GX channels are the transceiver channels that run at datarates ≤ 17.4 Gbps.

40 Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that require 1.12 V ± 20 mV, VCCR_GXB and VCCT_GXB = 1.12 V ± 20 mV.

41 Stratix 10 transceivers can support data rates below 1 Gbps through over sampling.

42 GXT channels are the transceiver channels that run at datarates ≤ 28.3 Gbps.

Table 32. H-Tile Fractional PLL Performance—Preliminary

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	6.25	GHz
	Minimum Frequency	500	MHz

Table 33. H-Tile CMU PLL Performance—Preliminary

Symbol/Description	Condition	All Transceiver Speed Grades	Unit
Supported Output Frequency	Maximum Frequency	5.15625	GHz
	Minimum Frequency	2450	MHz

1.2.2.2 Transceiver Specifications for GX/SX H-Tile Devices

Table 34. H-Tile Reference Clock Specifications—Preliminary

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported I/O Standards	Dedicated reference clock pin	CML, Differential LVPECL, LVDS, and HCSL			
	RX reference clock pin	CML, Differential LVPECL, and LVDS			
Input Reference Clock Frequency (CMU PLL)		61	—	800	MHz
Input Reference Clock Frequency (ATX PLL)		100	—	800	MHz
Input Reference Clock Frequency (fPLL PLL)		50 [43]	—	800	MHz
Rise time	20% to 80%	—	—	400	ps
Fall time	80% to 20%	—	—	400	ps
Duty cycle	—	45	—	55	%
Spread-spectrum modulating clock frequency	PCIe	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	%
On-chip termination resistors	—	—	100	—	Ω

continued...

43 The f_{MIN} is 29 MHz when the fPLL is used as a core PLL.

Symbol/Description	Condition	Min	Typ	Max	Unit
Absolute V_{MAX}	Dedicated reference clock pin	—	—	1.6	V
	RX reference clock pin	—	—	1.2	V
Absolute V_{MIN}	—	–0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	mV
V_{ICM} (AC coupled)	V_{CCR_GXB} =1.03 V	—	1.03	—	V
	V_{CCR_GXB} = 1.12 V	—	1.12	—	V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) [44]	100 Hz	—	—	–70	dBc/Hz
	1 kHz	—	—	–90	dBc/Hz
	10 kHz	—	—	–100	dBc/Hz
	100 kHz	—	—	–110	dBc/Hz
	≥ 1 MHz	—	—	–120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz)	1.5 to 100 MHz (PCIe)	—	—	4.2	ps (rms)
R_{REF}	—	—	2.0 k ±1%	—	Ω
$T_{SSC\text{-}MAX\text{-}PERIOD\text{-}SLEW}$	Max SSC df/dt			0.75	

44 To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

Table 35. H-Tile Transceiver Clock Network Maximum Data Rate Specifications—Preliminary

Clock Network	Maximum Performance [45]			Channel Span	Unit
	ATX	fPLL	CMU		
x1	17.4	12.5	10.3125	6 channels	Gbps
x6	17.4	12.5	N/A	6 channels	Gbps
x24	16	12.5	N/A	2 banks up and 2 banks down	Gbps
GXT clock lines	28.3	N/A	N/A	4 GXT channels within the same transceiver bank and 2 from the bank above or 2 from the bank below. [46]	Gbps

Table 36. H-Tile Receiver Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O, CML, Differential LVPECL, and LVDS			
Absolute V_{MAX} for a receiver pin [47]	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin [47]	—	-0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration [48]	—	—	—	1.6	V

continued...

45 The maximum data rate depends on speed grade.

46 If the upper ATX PLL in a bank is used, then the channel span includes two GXT channels from the bank above. If the lower ATX PLL in a bank is used, then the channel span includes two channels from the bank below.

47 The device cannot tolerate prolonged operation at this absolute maximum.

48 DC coupling specifications are pending silicon characterization.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration [48]	V_{CCR_GXB} = 1.03 V, 1.12 V [49], [52]	—	—	2.0	V
Minimum differential eye opening at receiver serial input pins [50]	—	50	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{ICM} (AC and DC coupled) [51]	V_{CCR_GXB} = 1.03 V [52]	—	700	—	mV
	V_{CCR_GXB} = 1.12 V [52]	—	750	—	mV
t_{LTR} [53]	—	—	—	1	ms
t_{LTD} [54]	—	4	—	—	µs
t_{LTD_manual} [55]	—	4	—	—	µs

continued...

49 Bonded channels operating at data rates above 16 Gbps require 1.12 V ± 20 mV at the pin. For channels that are placed in the same side of the device as the channels that required 1.12 V ± 20 mV, V_{CCR_GXB} = 1.12 V ± 20 mV.

50 The differential eye opening specification at the receiver input pins assumes that Receiver Equalization is disabled. If you enable Receiver Equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

51 Stratix 10 devices support DC coupling to other Stratix 10 devices and other devices operating under the Hybrid Memory Cube (HMC) specifications.

52 For GXT channels, V_{CCR_GXB} must be 1.12 V. For GX channels, V_{CCR_GXB} must be 1.03 V. V_{CCR_GXB} must be 1.12 V for the transceiver on the side of the device when using GX and GXT channels together.

53 t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

54 t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
$t_{LTR\_LTD\_manual}$ [56]	—	15	—	—	µs
Run Length	—	—	—	200	UI
CDR PPM tolerance	PCIe-only	-300	—	300	PPM
	All other protocols	-1000	—	1000	PPM

Table 37. H-Tile Transmitter Specifications—Preliminary

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O [57]			—
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	Ω
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.03 V [58]	—	515	—	mV
V_{OCM} (AC coupled)	V_{CCT_GXB} = 1.12 V [58]	—	560		mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.03 V [58]	—	515	—	mV
V_{OCM} (DC coupled)	V_{CCT_GXB} = 1.12 V [58]	—	560	—	mV

continued...

55 t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

56 $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

57 High Speed Differential I/O is the dedicated I/O standard for the transmitter in Stratix 10 transceivers.

58 For GXT channels, V_{CCT_GXB} must be 1.12 V. For GX channels, V_{CCT_GXB} must be 1.03 V. V_{CCT_GXB} must be 1.12 V for the transceiver bank when using GX and GXT channels together within the same bank.

Symbol/Description	Condition	Transceiver Speed Grade 3			Unit
		Min	Typ	Max	
Rise time [59]	20% to 80%	20	—	130	ps
Fall time [59]	80% to 20%	20	—	130	ps
Intra-differential pair skew	TX V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	ps

Table 38. H-Tile Typical Transmitter V_{OD} Settings—Preliminary

Symbol	V_{OD} Setting	V_{OD}/V_{CCT_GXB} Ratio
V_{OD} differential value = V_{OD}/V_{CCT_GXB} ratio x V_{CCT_GXB}	31	1.00
	30	0.97
	29	0.93
	28	0.90
	27	0.87
	26	0.83
	25	0.80
	24	0.77
	23	0.73
	22	0.70
	21	0.67
	20	0.63
	19	0.60
	18	0.57
	17	0.53
	16	0.50

continued...

59 The Quartus Prime software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Symbol	V_{OD} Setting	V_{OD}/V_{CCT_GXB} Ratio
	15	0.47
	14	0.43
	13	0.40
	12	0.37

Table 39. H-Tile Transmitter Channel-to-channel Skew Specifications—Preliminary

Mode	Channel Span	Maximum Skew	Unit
x6 Clock	Up to 6 channels in one bank	61	ps

Table 40. Transceiver Clocks Specifications for Stratix 10 GX/SX H-Tile Devices—Preliminary

Clock	Value	Unit
`reconfig_clk`	≤ 125	MHz
`fixed_clk` for the RX detect circuit	250 ± 20%	MHz

For OSC_CLK_1 specifications, refer to the External Configuration Clock Source Requirements section.

Related Links

External Configuration Clock Source Requirements on page 49

1.2.3 E-Tile Transceiver Performance Specifications

1.2.3.1 Transceiver Performance for Stratix 10 E-Tile Devices

Table 41. E-Tile Transmitter and Receiver Data Rate Performance Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Supported datarate[60]	NRZ	1		30	Gbps
	PAM-4	2		56[61]	Gbps

1.2.3.2 Transceiver Reference Clock Specifications

Table 42. E-Tile Reference Clock Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
I/O standard		LVPECL			
Termination voltage (Vtt)	2.5 V compliant	0.4	0.5	0.6	V
	3.3 V tolerant	1.04	1.3	1.56	V
Termination resistor (Rtt)		40	50	60	ohm
Differential voltage (Vdiff)		0.4	0.8	1.2	V
Input common mode voltage (Vcm)	2.5 V compliant, no internal termination resister	Vdiff/2		VCCN2P5V_IO-Vdiff/2	V
	2.5 V compliant, internal termination resister	VCCN2P5V_IO-1.6	VCCN2P5V_IO-1.3	VCCN2P5V_IO-1	V
	3.3 V tolerant, no internal termination resister	Vdiff/2		VCCN2P5V_IO-Vdiff/2	V
	3.3 V tolerant, internal termination resister	1.4	2	2.6	V
Absolute voltage		-0.5		2.8	V

60 The supported datarate is for chip-to-chip and backplane links.

61 Two channels are combined to support up to 56 Gbps.

1.2.3.3 Transmitter Specifications for Stratix 10 E-Tile Devices

Table 43. E-Tile Transmitter Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Transmitter differential output voltage peak-to-peak	No precursor/postcursor de-emphasis		0.965		V
Transmiter commom mode voltage			$V_{CCERT}/2$		V

1.2.3.4 Receiver Specifications for Stratix 10 E-Tile Devices

Table 44. E-Tile Receiver Specifications—Preliminary

Symbol/Description	Condition	Minimum	Typical	Maximum	Unit
Receiver run length[62]				100[63]	symbols
DC input impedance		40		60	ohm
DC differential input impedance		80	100	120	ohm
Powered down DC input impedance	Receiver pin impendance when the receiver termination is powered down	100k			ohm
Electrical Idle detection voltage	-	65		175	mV
Differential termination	From DC to 100 Mhz	80	100	120	ohm
PPM tolerance	Allowed frequency mismatch between REFCLK and RX data			750	ppm

62 No additional transition density requirements apply.

63 The incoming data must be statistically DC-balanced.

1.2.4 Core Performance Specifications

1.2.4.1 Clock Tree Specifications

Table 45. Clock Tree Performance for Stratix 10 Devices—Preliminary

Parameter	Performance			Unit
	–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
Programmable clock routing	1,100	900	780	MHz

1.2.4.2 PLL Specifications

1.2.4.2.1 Fractional PLL Specifications

Table 46. Fractional PLL Specifications for Stratix 10 Devices—Preliminary

These specifications are applicable when fPLL is used in core mode.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	—	29	—	800 [64]	MHz
f_{INPFD}	Input clock frequency to the phase frequency detector (PFD)	—	29	—	700	MHz
f_{VCO}	PLL voltage-controlled oscillator (VCO) operating range for transceiver applications	—	6	—	12.5	GHz
	PLL voltage-controlled oscillator (VCO) operating range for core applications	—	4.3	—	12.5	GHz
$t_{EINDUTY}$	Input clock duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock	—	—	—	1	GHz
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `reconfig_clk`	—	—	—	125	MHz

continued...

64 This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `pll_powerdown`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
f_{CLBW}	PLL closed-loop bandwidth	—	0.3	—	4	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	Non-SmartVID	—	—	±50	ps
		SmartVID	—	—	±75	ps
t_{ARESET}	Minimum pulse width on the `pll_powerdown` signal	—	10	—	—	ns
t_{INCCJ} [65], [66]	Input clock cycle-to-cycle jitter	F_{REF} ≥ 100 MHz	—	—	0.13	UI (p-p)
		F_{REF} < 100 MHz	—	—	650	ps (p-p)
t_{OUTPJ} [67]	Period jitter for clock output	F_{OUT} ≥ 100 MHz	—	—	600	ps (p-p)
		F_{OUT} < 100 MHz	—	—	60	mUI (p-p)
t_{OUTCCJ} [67]	Cycle-to-cycle jitter for clock output	F_{OUT} ≥ 100 MHz	—	—	600	ps (p-p)
		F_{OUT} < 100 MHz	—	—	60	mUI (p-p)
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	—	32	—	bit

Related Links

Memory Output Clock Jitter Specifications on page 48
Provides more information about the external memory interface clock output jitter specifications.

65 A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

66 F_{REF} is f_{IN}/N, specification applies when N = 1.

67 External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Stratix 10 Devices table.

1.2.4.2.2 I/O PLL Specifications

Table 47. I/O PLL Specifications for Stratix 10 Devices—Preliminary

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	–1 speed grade	10	—	1,100 [68]	MHz
		–2 speed grade	10	—	900 [68]	MHz
		–3 speed grade	10	—	750 [68]	MHz
f_{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f_{VCO}	PLL VCO operating range	–1 speed grade	600	—	1,600	MHz
		–2 speed grade	600	—	1,434	MHz
		–3 speed grade	600	—	1,250	MHz
f_{CLBW}	PLL closed-loop bandwidth	—	0.5	—	10	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f_{OUT}	Output frequency for internal clock (C counter)	–1 speed grade	—	—	1,100	MHz
		–2 speed grade	—	—	900	MHz
		–3 speed grade	—	—	750	MHz
f_{OUT_EXT}	Output frequency for external clock output	–1 speed grade	—	—	800	MHz
		–2 speed grade	—	—	720	MHz
		–3 speed grade	—	—	650	MHz
$t_{OUTDUTY}$	Duty cycle for dedicated external clock output (when set to 50%)	Non-SmartVID	45	50	55	%
		SmartVID	42	50	58	%
t_{FCOMP}	External feedback clock compensation time	—	—	—	5	ns

continued...

68 This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$f_{DYCONFIGCLK}$	Dynamic configuration clock for `mgmt_clk` and `scanclk`	—	—	—	200	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	—	10	—	—	ns
t_{INCCJ} [6970]	Input clock cycle-to-cycle jitter	$F_{REF} \geq 100$ MHz	—	—	0.15	UI (p-p)
		$F_{REF} < 100$ MHz	—	—	750	ps (p-p)
t_{OUTPJ_DC}	Period jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTPJ_IO} [71]	Period jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
t_{OUTCCJ_IO} [71]	Cycle-to-cycle jitter for clock output on the regular I/O	$F_{OUT} \geq 100$ MHz	—	—	600	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	60	mUI (p-p)
$t_{CASC\_OUTPJ\_DC}$	Period jitter for dedicated clock output in cascaded PLLs	$F_{OUT} \geq 100$ MHz	—	—	175	ps (p-p)
		$F_{OUT} < 100$ MHz	—	—	17.5	mUI (p-p)

69 A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

70 F_{REF} is f_{IN}/N, specification applies when $N = 1$.

71 External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Stratix 10 Devices table.

Related Links

Memory Output Clock Jitter Specifications on page 48
Provides more information about the external memory interface clock output jitter specifications.

1.2.4.3 DSP Block Specifications

Table 48. DSP Block Performance Specifications for Stratix 10 Devices—Preliminary

Mode	Performance			Unit
	–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	
Fixed-point 18 × 19 multiplication mode	1,000	771	667	MHz
Fixed-point 27 × 27 multiplication mode	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder mode	1,000	771	667	MHz
Fixed-point 18 × 18 multiplier adder summed with 36-bit input mode	1,000	771	667	MHz
Fixed-point 18 × 19 systolic mode	1,000	771	667	MHz
Complex 18 × 19 multiplication mode	1,000	771	667	MHz
Floating point multiplication mode	750	579	500	MHz
Floating point adder or subtract mode	750	579	500	MHz
Floating point multiplier adder or subtract mode	750	579	500	MHz
Floating point multiplier accumulate mode	750	579	500	MHz
Floating point vector one mode	750	579	500	MHz
Floating point vector two mode	750	579	500	MHz

1.2.4.4 Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Table 49. Memory Block Performance Specifications for Stratix 10 Devices—Preliminary

Memory	Mode	Performance			
		–E1V, –I1V	–E2V, –E2L, –I2V, –I2L	–E3V, –E3X, –I3V, –I3X	Unit
MLAB	Single port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port, all supported widths (×16/×32)	1,000	782	667	MHz
	Simple dual-port with read-during-write option	550	450	400	MHz
	ROM, all supported width (×16/×32)	1,000	782	667	MHz
M20K Block	Single-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, all supported widths	1,000	782	667	MHz
	Simple dual-port, coherent read enabled	1,000	782	667	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	800	640	560	MHz
	Simple dual-port with ECC enabled, 512 × 32	600	480	420	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	1,000	782	667	MHz
	True dual port, all supported widths	600	480	420	MHz
	Simple quad-port, all supported widths	600	480	420	MHz
	ROM, all supported widths	1,000	782	667	MHz
eSRAM	Simple dual-port	500–750	500–700	500–640	MHz

1.2.4.5 Internal Temperature Sensing Diode Specifications

Table 50. Internal Temperature Sensing Diode Specifications for Stratix 10 Devices—Preliminary

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40 to 125 °C	±5 °C	No	1 KSPS	< 5 ms	11 bits	11 bits

1.2.4.6 Internal Voltage Sensor Specifications

Table 51. Internal Voltage Sensor Specifications for Stratix 10 Devices—Preliminary

Parameter		Minimum	Typical	Maximum	Unit
Resolution		—	8	—	Bit
Sampling rate		—	—	1.0 [72]	KSPS
Differential non-linearity (DNL)		—	—	±1	LSB
Integral non-linearity (INL)		—	—	±1	LSB
Input capacitance		—	—	40	pF
Clock frequency		—	—	550	MHz
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.5	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.25	V

1.2.5 Periphery Performance Specifications

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

1.2.5.1 High-Speed I/O Specifications

Table 52. High-Speed I/O Specifications for Stratix 10 Devices—Preliminary

When serializer/deserializer (SERDES) factor J = 3 to 10, use the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

72 Pending silicon characterization.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards		Clock boost factor W = 1 to 40 [73]	10	—	800	10	—	700	10	—	625	MHz
f_{HSCLK_in} (input clock frequency) Single-Ended I/O Standards		Clock boost factor W = 1 to 40 [73]	10	—	625	10	—	625	10	—	525	MHz
f_{HSCLK_OUT} (output clock frequency)		—	—	—	800 [74]	—	—	700 [74]	—	—	625 [74]	MHz
Transmitter	True Differential I/O Standards - f_{HSDR} (data rate) [75]	SERDES factor J = 4 to 10 [767877]	[78]	—	1600 [79]	[78]	—	1434 [79]	[78]	—	1250 [79]	Mbps
		SERDES factor J = 3 [767877]	[78]	—	[79]	[78]	—	[79]	[78]	—	[79]	Mbps
		SERDES factor J = 2, uses DDR registers	[78]	—	840 [7980]	[78]	—	[7980]	[78]	—	[7980]	Mbps
		SERDES factor J = 1, uses DDR registers	[78]	—	420 [7980]	[78]	—	[7980]	[78]	—	[7980]	Mbps

continued...

73 Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.

74 This is achieved by using the PHY clock network.

75 Requires package skew compensation with PCB trace length.

76 The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

77 The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.

78 The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.

79 Pending silicon characterization.

80 The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	$t_{x\ Jitter}$ - True Differential I/O Standards	Total jitter for data rate, 600 Mbps – 1.6 Gbps	—	—	160	—	—	200	—	—	250	ps
		Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.12	—	—	0.15	UI
	t_{DUTY} [81]	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
	t_{RISE} & t_{FALL} [7782]	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	ps
	TCCS [8175]	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 [767877]	—	—	1600	—	—	1434	—	—	1250	Mbps
		SERDES factor J = 3 [767877]	—	—	[79]	—	—	[79]	—	—	[79]	Mbps
	f_{HSDR} (data rate) (without DPA) [75]	SERDES factor J = 3 to 10	[78]	—	[83]	[78]	—	[83]	[78]	—	[83]	Mbps
		SERDES factor J = 2, uses DDR registers	[78]	—	[80]	[78]	—	[80]	[78]	—	[80]	Mbps
		SERDES factor J = 1, uses DDR registers	[78]	—	[80]	[78]	—	[80]	[78]	—	[80]	Mbps
DPA (FIFO mode)	DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI

continued...

81 Not applicable for DIVCLK = 1.

82 This applies to default pre-emphasis and V_{OD} settings only.

83 You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Symbol		Condition	–E1V, –I1V			–E2V, –E2L, –I2L, –I2V			–E3V, –E3X, –I3X, –I3V			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	UI
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	± ppm
Non DPA mode	Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

1.2.5.2 DPA Lock Time Specifications

Figure 2. DPA Lock Time Specifications with DPA PLL Calibration Enabled

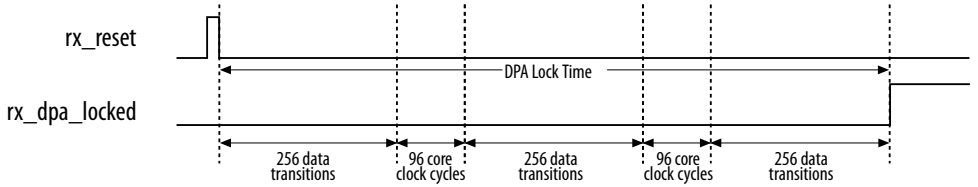


Table 53. DPA Lock Time Specifications for Stratix 10 Devices—Preliminary

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions [84]	Maximum Data Transition
SPI-4	00000000001111111111	2	128	640
Parallel Rapid I/O	00001111	2	128	640

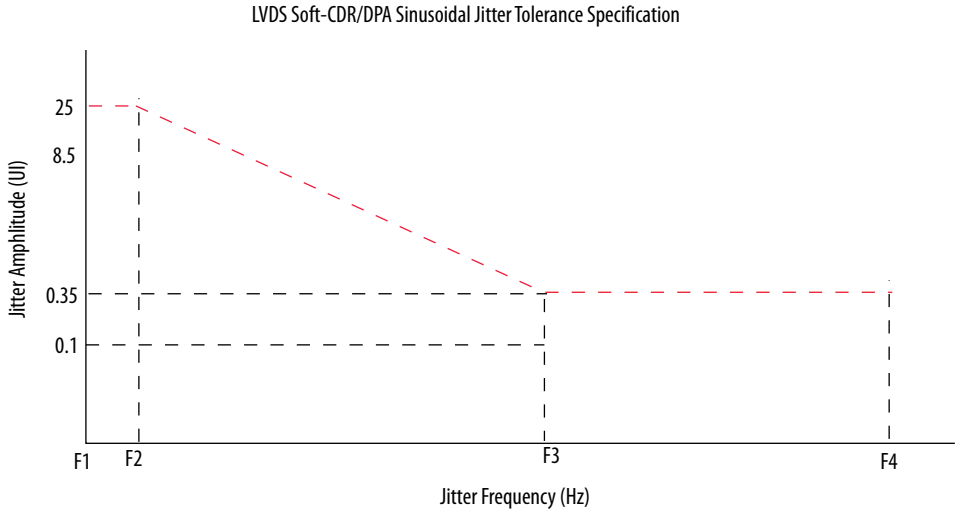
continued...

84 This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions [84]	Maximum Data Transition
	10010000	4	64	640
Miscellaneous	10101010	8	32	640
	01010101	8	32	640

1.2.5.3 LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

Figure 3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

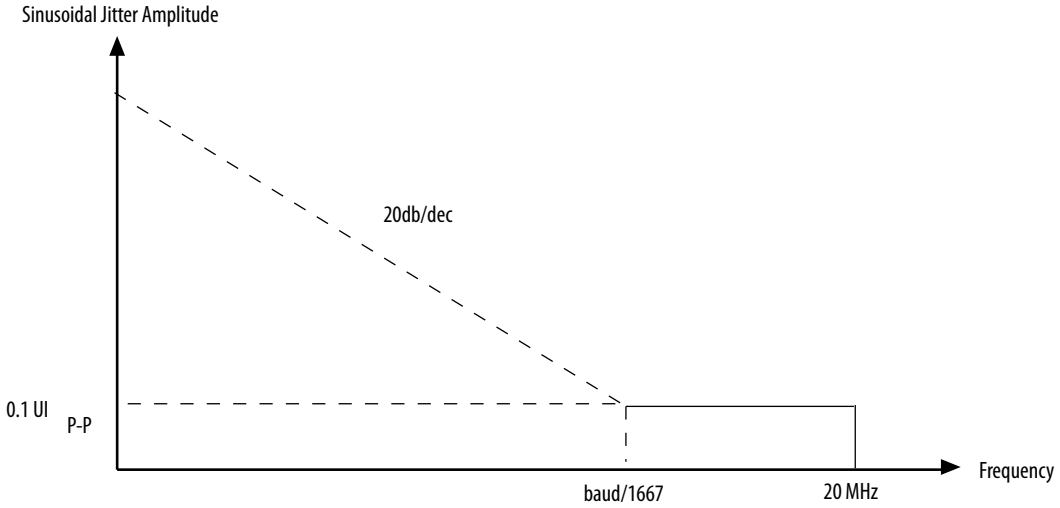


84 This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Table 54. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps—Preliminary

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.35
F4	50,000,000	0.35

Figure 4. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



1.2.5.4 DLL Range Specifications

Table 55. DLL Frequency Range Specifications for Stratix 10 Devices—Preliminary

Stratix 10 devices support memory interface frequencies lower than 667 MHz, although the reference clock that feeds the DLL must be at least 667 MHz. To support interfaces below 667 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range.

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1,333	MHz

1.2.5.5 DQS Logic Block Specifications

Table 56. DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix 10 Devices—Preliminary

This error specification is the absolute maximum and minimum error.

Symbol	Performance			Unit
	–1 Speed Grade	–2 Speed Grade	–3 Speed Grade	
t_{DQS_PSERR}	4	6	8	ps

1.2.5.6 Memory Output Clock Jitter Specifications

Table 57. Memory Output Clock Jitter Specifications for Stratix 10 Devices—Preliminary

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory output clock jitter is applicable when an input jitter of 10 ps peak-to-peak is applied with bit error rate (BER) 10^{-12}, equivalent to 14 sigma.

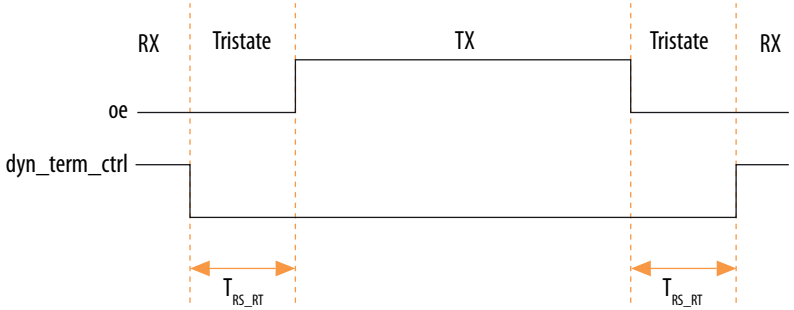
Clock Network	Parameter	Symbol	Performance			Unit
			–1 Speed Grade	–2 Speed Grade	–3 Speed Grade	
PHY clock	Clock period jitter	$t_{JIT(per)}$	58	58	58	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	58	58	58	ps
	Duty cycle jitter	$t_{JIT(duty)}$	58	58	58	ps

1.2.5.7 OCT Calibration Block Specifications

Table 58. OCT Calibration Block Specifications for Stratix 10 Devices—Preliminary

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	> 2000	—	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	TBD	—	ns

Figure 5. Timing Diagram for on oe and dyn_term_ctrl Signals



1.3 Configuration Specifications

1.3.1 External Configuration Clock Source Requirements

Table 59. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements—Preliminary

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency [85]	Powered by V_{CCIO_SDM}		25/100/125		MHz
Clock input jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

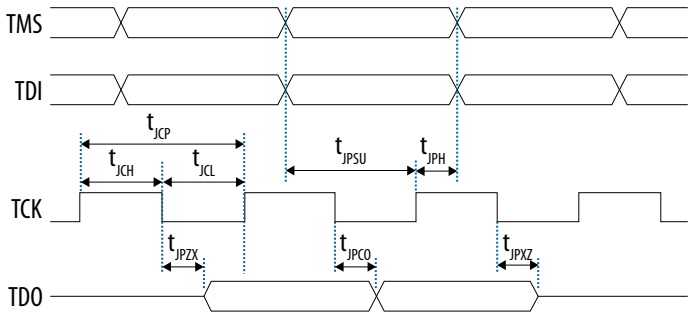
85 The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. Other frequencies in the range are not supported.

1.3.2 JTAG Configuration Timing

Table 60. JTAG Timing Parameters and Values for Stratix 10 Devices—Preliminary

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t_{JCP}	TCK clock period	30, 167 [86]	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	7	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14	ns

Figure 6. JTAG Timing Diagram



86 The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.8 V when you perform the volatile key programming.

1.3.3 AS Configuration Timing

Table 61. AS Timing Parameters for Stratix 10 Devices—Preliminary

Intel recommends performing trace length matching for nCS0 and AS_DATA pins to AS_CLK to minimize the skew. The maximum tolerance for skew between nCS0 and AS_CLK is less than 200 ps. The tolerance for skew between AS_DATA and AS_CLK ranges between 200 ps – 400 ps.

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk}	AS_CLK clock period	7.52	—	—	ns
$T_{dutycycle}$	AS_CLK duty cycle	45	50	55	%
T_{dcsfrs}	AS_nCSO[3:0] asserted to first AS_CLK edge	4.21 [87]	—	6.05 [87]	ns
T_{dcslst}	Last AS_CLK edge to AS_nCSO[3:0] deasserted	5.18 [87]	—	7.03 [87]	ns
T_{do}	AS_DATA0 output delay	0	—	2.6	ns
T_{ext_delay} [88]	Total external propagation delay on AS signals	0	—	15	ns
T_{ext_skew}	Skew delay for AS_DATA signals	—	—	2	ns
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	1	—	—	AS_CLK

87 AS operating at maximum clock frequency = 133 MHz. The delay is larger when operating at AS clock frequency lower than 133 MHz.

88 Text_delay = Tbd_clk + Tco + Tbd_data + Tadd
Tbd_clk: Propagation delay for AS_CLK between FPGA and flash device.
Tco: Output hold time of flash device.
Tbd_data: Propagation delay for AS_DATA bus between FPGA and flash device.
Tadd: Propagation delay for active/passive components on AS_DATA interfaces.

Figure 7. AS Configuration Serial Output Timing Diagram

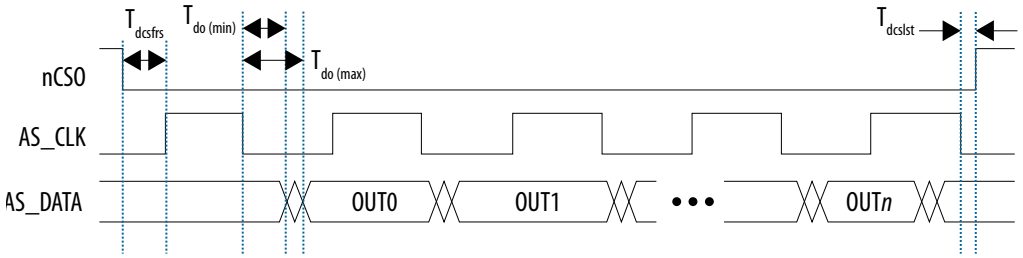
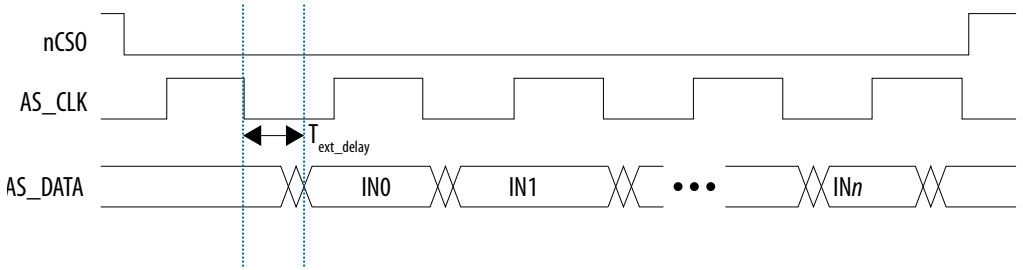


Figure 8. AS Configuration Serial Input Timing Diagram



1.3.4 Avalon-ST Configuration Timing

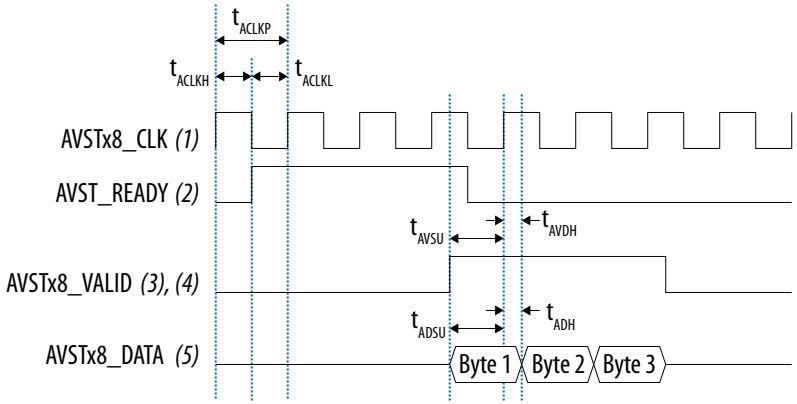
Table 62. Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Stratix 10 Devices—Preliminary

Symbol	Description	Minimum	Maximum	Unit
t_{ST0}	nSTATUS low pulse during configuration error	0.5	1.5	ms
t_{ACLKH}	AVST_CLK high time	3.6	—	ns
t_{ACLKL}	AVST_CLK low time	3.6	—	ns
t_{ACLKP}	AVST_CLK period	8	—	ns
t_{ADSU} [89]	AVST_DATA setup time before rising edge of AVST_CLK	5.5	—	ns

continued...

Symbol	Description	Minimum	Maximum	Unit
t_{ADH} [89]	AVST_DATA hold time after rising edge of AVST_CLK	0	—	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	5.5	—	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	—	ns

Figure 9. Avalon-ST Configuration Timing Diagram



Notes:
1. For Avalon-ST x16 and x32, this signal is AVST_CLK.
2. AVST_READY is valid only when nSTATUS is high. AVST_READY is an asynchronous signal to AVSTx8_CLK.
3. For Avalon-ST x16 and x32, this signal is AVST_VALID.
4. The waveforms shows the interface signals with a host which uses ready latency =2. The AVSTx8_VALID signal is delayed from AVST_READY signal by 2 clock cycles.
5. For Avalon-ST x16 and x32, this signal is AVST_DATA[15:0] and AVST_DATA[31:0] respectively.

89 Data sampled by the FPGA (sink) at the next rising clock edge.

1.3.5 NAND Configuration Timing

Table 63. NAND ONFI 1.0 Mode 0-5 Timing Requirements for Stratix 10 Devices—Preliminary

Symbol	Description	Minimum	Maximum	Unit
t_{WP}	Write enable pulse width	10	—	ns
t_{WH}	Write enable hold time	7	—	ns
t_{RP}	Read enable pulse width	10	—	ns
t_{REH}	Read enable hold time	7	—	ns
t_{CLS}	Command latch enable to write enable setup time	10	—	ns
t_{CLH}	Command latch enable to write enable hold time	5	—	ns
t_{CS}	Chip enable to write enable setup time	15	—	ns
t_{CH}	Chip enable to write enable hold time	5	—	ns
t_{ALS}	Address latch enable to write enable setup time	10	—	ns
t_{ALH}	Address latch enable to write enable hold time	5	—	ns
t_{DS}	Data to write enable setup time	7	—	ns
t_{DH}	Data to write enable hold time	5	—	ns
t_{CEA}	Chip enable to data access time	—	100	ns
t_{REA}	Read enable to data access time	—	40	ns
t_{RHZ}	Read enable to data high impedance	—	200	ns
t_{RR}	Ready to read enable low	20	—	ns
t_{WB}	Write enable high to R/B low	—	200	ns

Figure 10. NAND Command Latch Timing Diagram

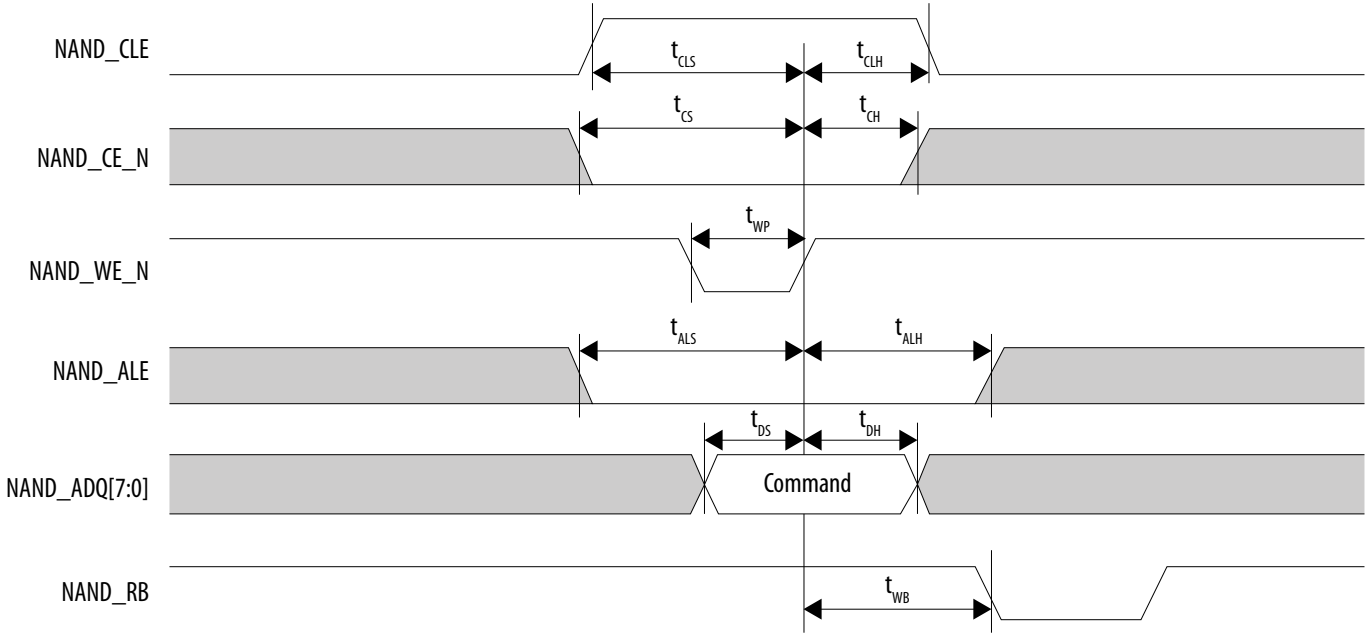


Figure 11. NAND Address Latch Timing Diagram

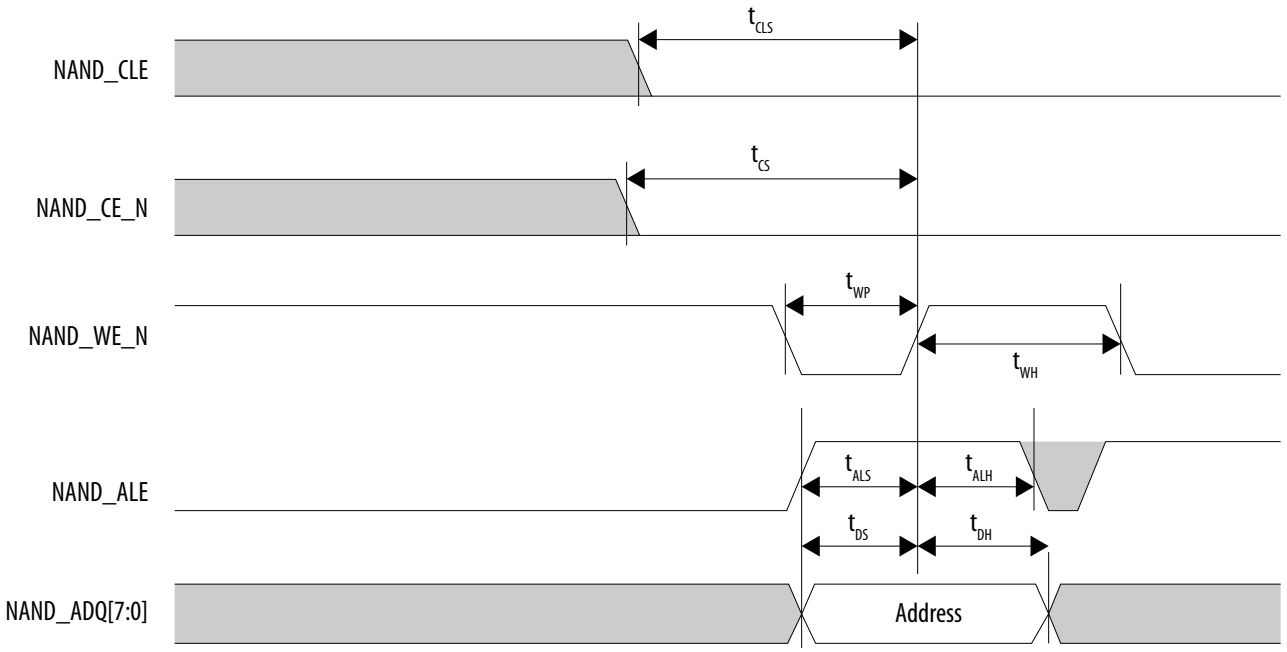


Figure 12. NAND Data Output Cycle Timing Diagram

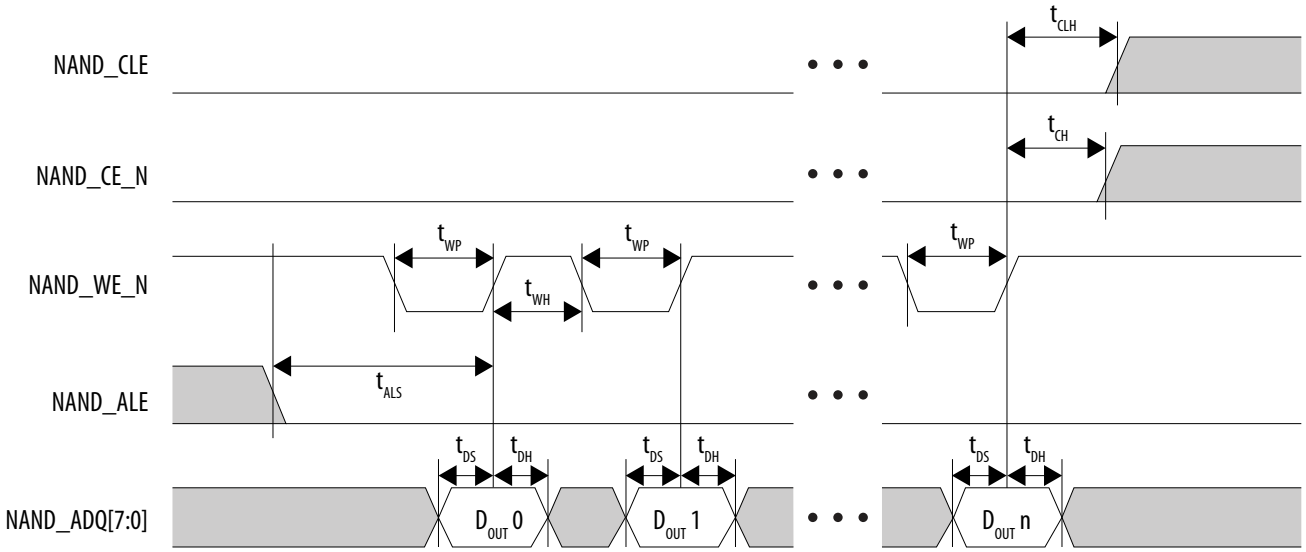


Figure 13. NAND Data Input Cycle Timing Diagram

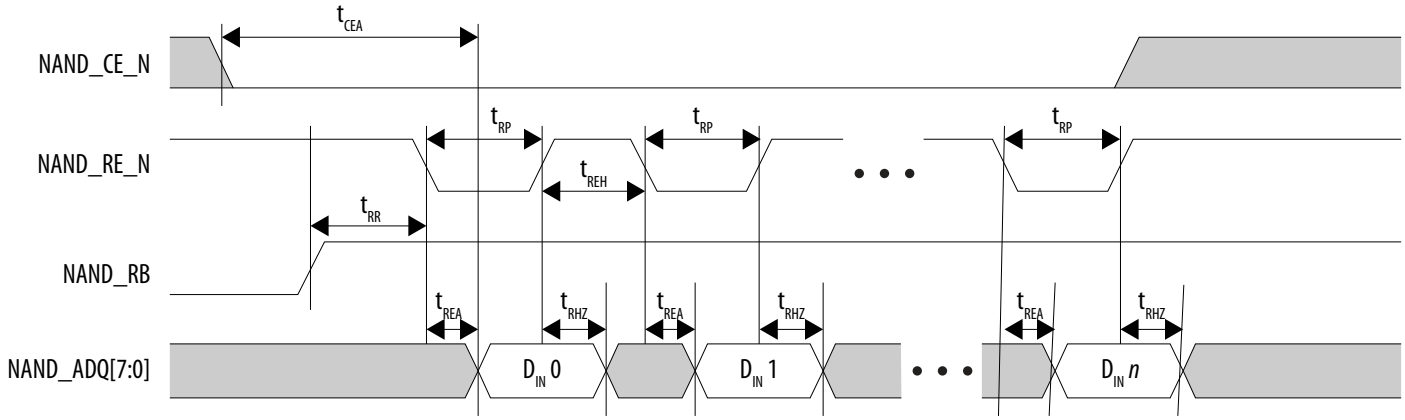


Figure 14. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

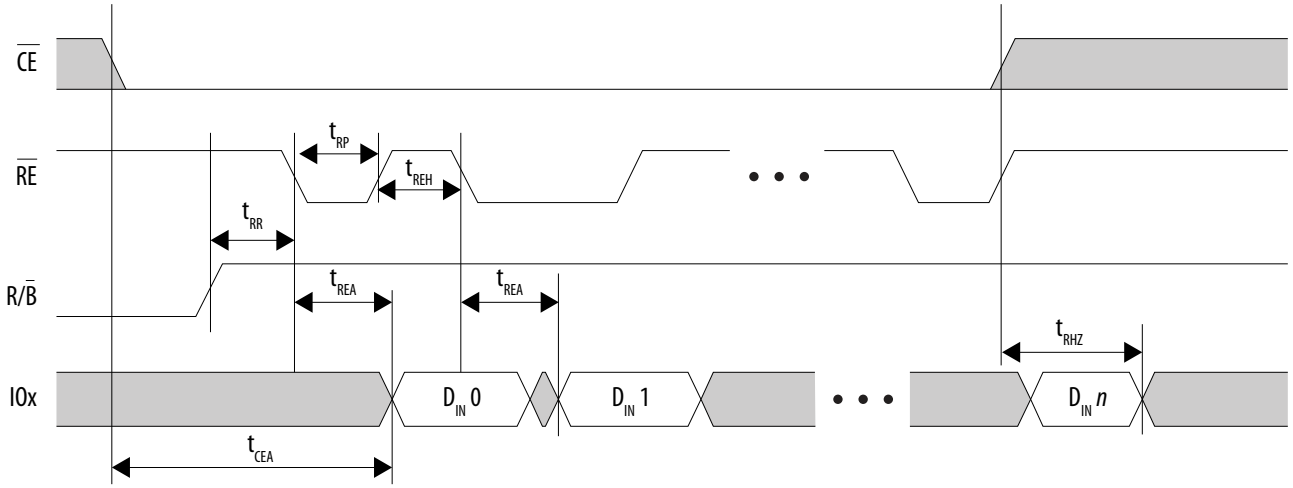


Figure 15. NAND Read Status Timing Diagram

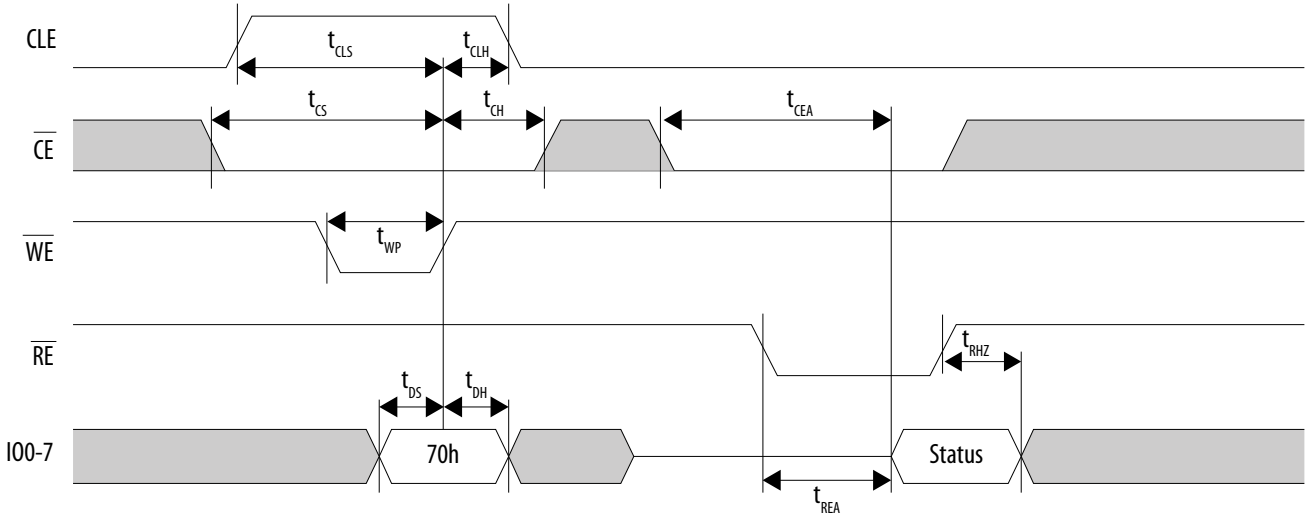
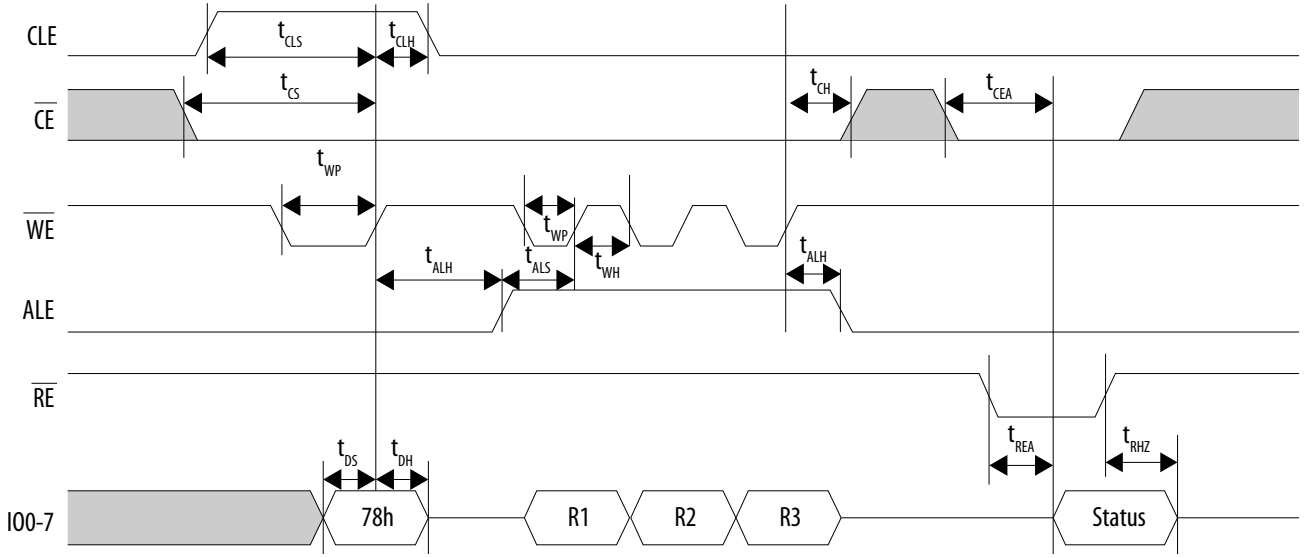


Figure 16. NAND Read Status Enhanced Timing Diagram

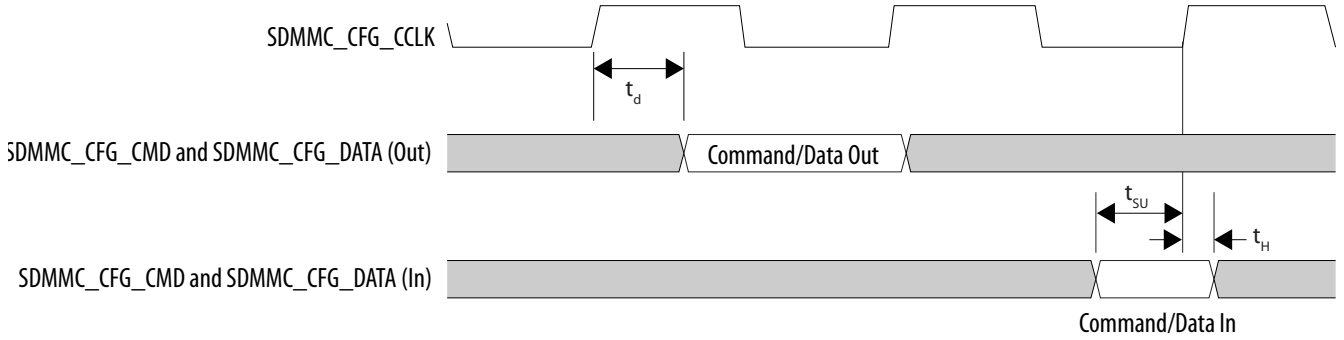


1.3.6 SD/MMC Configuration Timing

Table 64. SD/MMC Timing Parameters for Stratix 10 Devices—Preliminary

Symbol	Description	Minimum	Typical	Maximum	Unit
t_{SDCLKP}	SDMMC_CFG_CCLK clock period (Identification mode)	2,500	—	—	ns
	SDMMC_CFG_CCLK clock period (Standard SD mode)	40	—	—	ns
	SDMMC_CFG_CCLK clock period (High-speed SD mode)	20	—	—	ns
$t_{DUTYCYCLE}$	SDMMC_CFG_CCLK duty cycle	45	50	55	%
t_{SU}	SDMMC_CFG_CMD/SDMMC_CFG_DATA input setup	5	—	—	ns
t_H	SDMMC_CFG_CMD/SDMMC_CFG_DATA input hold	1	—	—	ns
t_d	SDMMC_CFG_CMD/SDMMC_CFG_DATA output delay	8.5	—	11	ns

Figure 17. SD/MMC Timing Diagram



1.3.7 Initialization

Table 65. Initialization Clock Source Option and the Maximum Frequency for Stratix 10 Devices—Preliminary

Configuration Scheme	Maximum duration required for initialization
AS, AVST ×8, AVST ×16, AVST ×32, NAND, SD/MMC	2 ms [90]

1.3.8 Configuration Bit Stream Sizes

Table 66. Configuration Bit Stream Sizes for Stratix 10 Devices—Preliminary

This table shows the estimated configuration bit stream sizes of the EPCQ-L serial configuration device or external flash size before design compilation. The sizes are for compressed bit stream. The actual sizes may vary based on your design.

Variant	Product Line	Compressed Configuration Bit Stream Size (Mbits)
Stratix 10 GX	GX 400, GX 650	79
	GX 850, GX 1100	133
	GX 1650, GX 2100	227
	GX 2500, GX 2800	336

continued...

90 This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.

Variant	Product Line	Compressed Configuration Bit Stream Size (Mbits)
	GX 4500, GX 5500	448
Stratix 10 SX	SX 400, SX 650	79
	SX 850, SX 1100	133
	SX 1650, SX 2100	227
	SX 2500, SX 2800	336
	SX 4500, SX 5500	448

1.3.9 Minimum Configuration Time Estimation

Hyper Initialization is an option that can be enabled or disabled through the setting in the Quartus Prime software to initialize or reset the HyperFlex registers to a known state at device configuration.

Table 67. Minimum Configuration Time Estimation for Stratix 10 Devices (JTAG and Avalon-ST)—Preliminary

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		JTAG		AVST ×8		AVST ×16		AVST ×32	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Stratix 10 GX	GX 400, GX 650	3000/3100	3000/3100	137/167	91/111	77/108	51/72	60/92	40/61
	GX 850, GX 1100	5300/5600	5300/5600	228/284	152/189	123/179	82/119	95/150	63/100
	GX 1650, GX 2100	9000/9500	9000/9500	377/426	251/284	197/248	131/165	107/158	71/105
	GX 2500, GX 2800	13300/14000	13300/14000	551/620	367/413	284/354	189/236	150/221	100/147
	GX 4500, GX 5500	17600/18700	17600/18700	723/831	482/554	371/480	247/320	194/303	129/202

continued...

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		JTAG		AVST ×8		AVST ×16		AVST ×32	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Stratix 10 SX	SX 400, SX 650	3000/3100	3000/3100	137/167	91/111	77/108	51/72	60/92	40/61
	SX 850, SX 1100	5300/5600	5300/5600	228/284	152/189	123/179	82/119	95/150	63/100
	SX 1650, SX 2100	9000/9500	9000/9500	377/426	251/284	197/248	131/165	107/158	71/105
	SX 2500, SX 2800	13300/14000	13300/14000	551/620	367/413	284/354	189/236	150/221	100/147
	SX 4500, SX 5500	17600/18700	17600/18700	723/831	482/554	371/480	247/320	194/303	129/202

Table 68. Minimum Configuration Time Estimation for Stratix 10 Devices (AS, NAND, and SD/MMC)—Preliminary

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		AS ×1		AS ×4		NAND		SD/MMC	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
Stratix 10 GX	GX 400, GX 650	1134/1260	756/840	284/315	189/210	366/396	244/264	366/396	244/264
	GX 850, GX 1100	1800/2022	1200/1348	450/506	300/337	597/653	398/435	597/653	398/435
	GX 1650, GX 2100	2862/3066	1908/2044	716/767	477/511	966/1017	644/678	966/1017	644/678

continued...

Variant	Product Line	Minimum Configuration Time (ms) [Hyper Initialization Off/Hyper Initialization On]							
		AS ×1		AS ×4		NAND		SD/MMC	
		170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)	170 – 230 MHz Internal Clock (Using Internal Clock Source)	250 MHz Internal Clock (Using External Clock Source)
	GX 2500, GX 2800	4116/4398	2744/2932	1029/1100	686/733	1403/1472	935/981	1403/1472	935/981
	GX 4500, GX 5500	5352/5796	3568/3864	1338/1449	892/966	1800/1950	1200/1300	1800/1950	1200/1300
Stratix 10 SX	SX 400, SX 650	1134/1260	756/840	284/315	189/210	366/396	244/264	366/396	244/264
	SX 850, SX 1100	1800/2022	1200/1348	450/506	300/337	597/653	398/435	597/653	398/435
	SX 1650, SX 2100	2862/3066	1908/2044	716/767	477/511	966/1017	644/678	966/1017	644/678
	SX 2500, SX 2800	4116/4398	2744/2932	1029/1100	686/733	1403/1472	935/981	1403/1472	935/981
	SX 4500, SX 5500	5352/5796	3568/3864	1338/1449	892/966	1800/1950	1200/1300	1800/1950	1200/1300

1.4 I/O Timing

The Quartus Prime Timing Analyzer provides accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

The I/O Timing specifications will be available in a future release of the *Stratix 10 Device Datasheet*.

1.5 Document Revision History

Date	Version	Changes
February 2017	2017.02.17	Made the following changes:

continued...

Date	Version	Changes
		• Added the "Transceiver Power Supply Operating Conditions for Stratix 10 GX/SX E-Tile Devices" table. • Added the "E-Tile Transceiver Performance Specifications" section. • Added the "Transceiver Performance forStratix 10 E-Tile Devices" section. • Added the "Transceiver Reference Clock Specifications" section. • Added the "Transmitter Specifications for Stratix 10 E-Tile Devices" section. • Added the "Receiver Specifications for Stratix 10 E-Tile Devices" section. • Updated the "AS Timing Parameters for Stratix 10 Devices" table. — Updated T_{dcsfrs} and T_{dcslst}. — Added T_{ext_delay} and T_{ext_skew}. — Removed T_{su} and T_{h}. • Updated AS Configuration Serial Input Timing Diagram.
December 2016	2016.12.09	Made the following changes: • Changed the max t_{LTR} value and unit of measure in the "L-Tile Receiver Specifications" table. • Made the following changes to the "Transceiver Clocks Specifications for Stratix 10 GX/SX L-Tile Devices" table: — Changed the value of the `reconfig_clk` signal — Added a new footnote to the GX channel — Changed the minimum values for the GXT channel • Changed the max t_{LTR} value and unit of measure in the "H-Tile Receiver Specifications" table. • Removed the QPI footnote from the "H-Tile Transmitter Specifications" table. • Changed the value of the `reconfig_clk` signal in the "Transceiver Clocks Specifications for Stratix 10 GX/SX H-Tile Devices" table. • Changed the minimum value of f_{INPFD} in the "Fractional PLL Specifications for Stratix 10 Devices" table.
October 2016	2016.10.31	Initial release.