Panasonic

AN44063A

37V/0.8A Stepping Motor Driver

FEATURES

- 4-phase input (W1-2phase excitation enabled; exclusive OR function incorporated for simultaneous-ON prevention)
- Built-in CR chopping (with frequency selected)
- Built-in thermal protection and low voltage detection circuit
- Built-in 5 V power supply
- 32 pin Plastic Shrink Small Outline Package (SSOP Type)

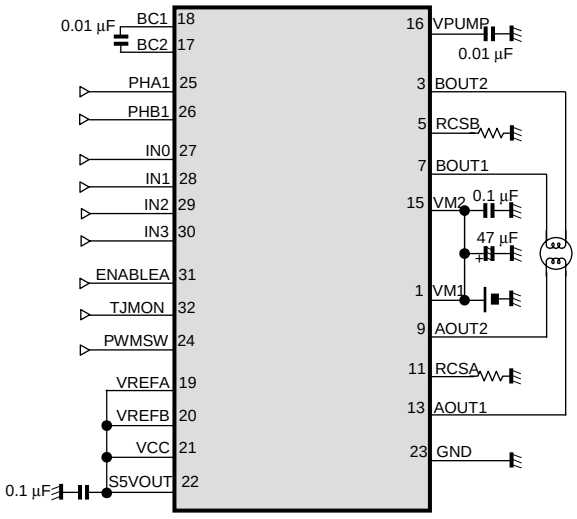
DESCRIPTION

AN44063A is a two channels H-bridge driver LSI.
Bipolar stepping motor can be controlled by a single driver LSI.
2-phase,1-2(type 2) phase, W1-2 phase can be selected.

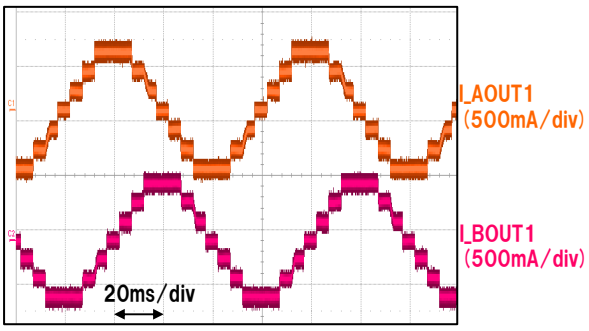
APPLICATIONS

- LSI for stepping motor drives

SIMPLIFIED APPLICATION



Motor Current Waveform



Condition:
VM=24V
Peak motor current:600mA
excitation mode :W1-2 phase drive

Notes)
This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage1 (Pin 1, 15)	V_M	37	V	*3
Supply voltage2 (Pin 21)	V_{CC}	– 0.3 to + 6	V	*3
Power dissipation	P_D	0.427	W	*1
Operating ambient temperature	T_{opr}	–20 to + 70	°C	*2
Operating junction temperature	T_j	–20 to + 150	°C	*2
Storage temperature	T_{stg}	–55 to + 150	°C	*2
Output pin voltage (Pin 3, 7, 9, 13)	V_{OUT}	37	V	*3
Motor drive current (Pin 3, 7, 9, 13)	I_{OUT}	± 0.8	A	*3
Flywheel diode current (Pin 3, 7, 9, 13)	I_f	0.8	A	*3
Input Voltage Range	V_{RCSA},V_{RCSB}	-0.5 to 1.5	V	—
	V_{VPUMP}	(VM-1) to 43	V	—
	V_{BC2}	(VM-1) to 43	V	—
	V_{BC1}	VM+0.3	V	—
	$V_{VREFA,}V_{VREFB}$	-0.3 to 6	V	—
	I_{S5VOUT}	-7 to 0	mA	—
	$V_{PHA1,}V_{PHB1}$	-0.3 to 6	V	—
	V_{PWMSW}	-0.3 to 6	V	—
	$V_{IN0\sim IN3}$	-0.3 to 6	V	—
	$V_{ENABLEA}$	-0.3 to 6	V	—
ESD	HBM (Human Body Model)	± 1	kV	—
	CDM (Charge Device Model)	± 1	kV	—

Notes). This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: The power dissipation shown is the value at T_a = 70°C for the independent (unmounted) LSI package without a heat sink. When using this LSI, refer to the P_D-T_a diagram of the package standard page 4 and use under the condition not exceeding the allowable value.

*2: Except for the storage temperature, operating ambient temperature, and power dissipation all ratings are for Ta = 25°C. Refer to the package power dissipation prepared else and use under the condition not exceeding the allowable value.

*3: Do not apply current or voltage from outside to any pin not listed above.
In the circuit current, (+) means the current flowing into LSI and (–) means the current flowing out of LSI.

POWER DISSIPATION RATING

Condition	θ_{JA}	PD (Ta=25 °C)	PD (Ta=70 °C)
Mount on PWB *1	96.9 °C/W	1290mW	825mW
Without PWB	187.1 °C/W	668mW	427mW

Note). For the actual usage, please refer to the PD-Ta characteristics diagram in the package specification, supply voltage, load and ambient temperature conditions to ensure that there is enough margin follow the power and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy: 50×50×0.8 (mm)

CAUTION

Although this has limited built-in ESD protection circuit, but permanent damage may occur on it. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VM1,VM2	16	24	34	V	*1
	V_{CC}	4.5	5	5.5	V	*1
Input Voltage Range	V_{PWMSW}	0	-	V_{CC}	V	—
	$V_{PHA1,}V_{PHB1}$	0	-	V_{CC}	V	—
	$V_{IN0\sim IN3}$	0	-	V_{CC}	V	—
	$V_{ENABLEA}$	0	-	V_{CC}	V	—
	$V_{VREFA,}V_{VREFB}$	0	-	5	V	—
External Constants	C_{BC}	-	0.01	-	µF	—
	C_{VPUMP}	-	0.01	-	µF	—
	C_{S5VOUT}	-	0.1	-	µF	—
Operating ambient temperature	Ta^{opr}	-20	-	70	°C	—
Operating junction temperature	Tj^{opr}	-	-	120	°C	—

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

ELECRTRICAL CHARACTERISTICS

VM=24V,T_a = 25°C±2°C unless otherwise noted.

*1 : Typical Value checked by design.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Output Drivers							
High-level output saturation voltage	V_{OH}	I = – 0.5 A	V_M– 0.47	V_M– 0.31	—	V	—
Low-level output saturation voltage	V_{OL}	I = 0.5 A	—	0.47	0.71	V	—
Flywheel diode forward voltage	V_{DI}	I = 0.5 A	0.5	1.0	1.5	V	—
Output leakage current	I_{LEAK}	V_M = V_{OUT} = 37 V, V_{RCS} = 0 V	—	10	50	µA	—
Supply current (with two circuits turned off)	I_M	ENABLEA = 5 V	—	4	6	mA	—
Output slew rate 1	VT_r	Rising edge	—	270	—	V/µs	*1
Output slew rate 2	VT_f	Falling edge	—	330	—	V/µs	*1
Dead time	T_D	—	—	2.8	—	µs	*1
I/O Block							
Supply current(with two circuits turned off)	I_{CC}	ENABLEA = 5 V	—	1.4	2.2	mA	—
High-level IN input voltage	V_{INH}	—	2.2	—	V_{CC}	V	—
Low-level IN input voltage	V_{INL}	—	0	—	0.6	V	—
High-level IN input current	I_{INH}	IN0 = IN1 = IN2 = IN3 = 5 V	–10	—	10	µA	—
Low-level IN input current	I_{INL}	IN0 = IN1 = IN2 = IN3 = 0 V	–15	—	15	µA	—
High-level PHA1/PHB1 input voltage	V_{PHAH} V_{PHBH}	—	2.2	—	V_{CC}	V	—
Low-level PHA1/PHB1 input voltage	V_{PHAL} V_{PHBL}	—	0	—	0.6	V	—
High-level PHA1/PHB1 input current	I_{PHAH} I_{PHBH}	PHA1 = PHB1 = 5 V	25	50	100	µA	—
Low-level PHA1/PHB1 input current	I_{PHAL} I_{PHBL}	PHA1 = PHB1 = 0 V	–15	—	15	µA	—
High-level ENABLEA input voltage	$V_{ENABLEAH}$	—	2.2	—	V_{CC}	V	—
Low-level ENABLEA input voltage	$V_{ENABLEAL}$	—	0	—	0.6	V	—
High-level ENABLEA input current	$I_{ENABLEAH}$	ENABLEA = 5 V	–10	—	10	µA	—
Low-level ENABLEA input current	$I_{ENABLEAL}$	ENABLEA = 0 V	–15	—	15	µA	—
High-level PWMSW input voltage	V_{PWMSWH}	—	2.2	—	V_{CC}	V	—
Low-level PWMSW input voltage	V_{PWMSWL}	—	0	—	0.6	V	—

ELECRTRICAL CHARACTERISTICS（continued）

VM=24V,T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I/O Block（Continued)							
High-level PWMSW input current	I_{PWMSWH}	PWMSW = 5 V	25	50	100	µA	—
Low-level PWMSW input current	I_{PWMSWL}	PWMSW = 0 V	–15	—	15	µA	—
Torque Control Block							
Input bias current	I_{REFA} I_{REFB}	V_{REFA} = 5 V V_{REFB} = 5 V	70	100	130	µA	—
PWM frequency1	f_{PWM1}	PWMSW = 0 V	34	52	70	kHz	—
PWM frequency2	f_{PWM2}	PWMSW = 5 V	17	26	35	kHz	—
Pulse blanking time	T_B	V_{REFA} = V_{REFB} = 0 V	0.38	0.75	1.12	µs	—
Cmp threshold H (100%)	VT_H	IN0 = IN1 = 0 V IN2 = IN3 = 0 V	475	500	525	mV	—
Cmp threshold C (67%)	VT_C	IN0 = 5 V, IN1 = 0 V IN2 = 5 V, IN3 = 0 V	308	333	359	mV	—
Cmp threshold L (33%)	VT_L	IN0 = 0 V, IN1 = 5 V IN2 = 0 V, IN3 = 5 V	151	167	184	mV	—
Reference Voltage Block							
Reference voltage	$V_{S5\ VOUT}$	$I_{S5\ VOUT}$ = – 2.5 mA	4.5	5.0	5.5	V	—
Output impedance	$Z_{S5\ VOUT}$	$I_{S5\ VOUT}$ = – 5 mA	—	18	27	Ω	—

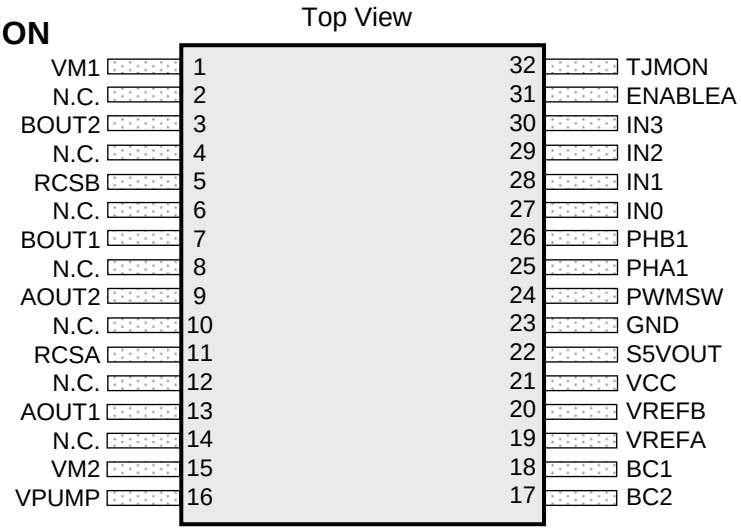
ELECRTRICAL CHARACTERISTICS（continued）

VM=24V,T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Thermal Protection							
Thermal protection operating temperature	TSD_{on}	—	—	150	—	°C	*1
Thermal protection hysteresis width	ΔTSD	—	—	40	—	°C	*1

Note) *1 : Typical Value checked by design.

PIN CONFIGURATION

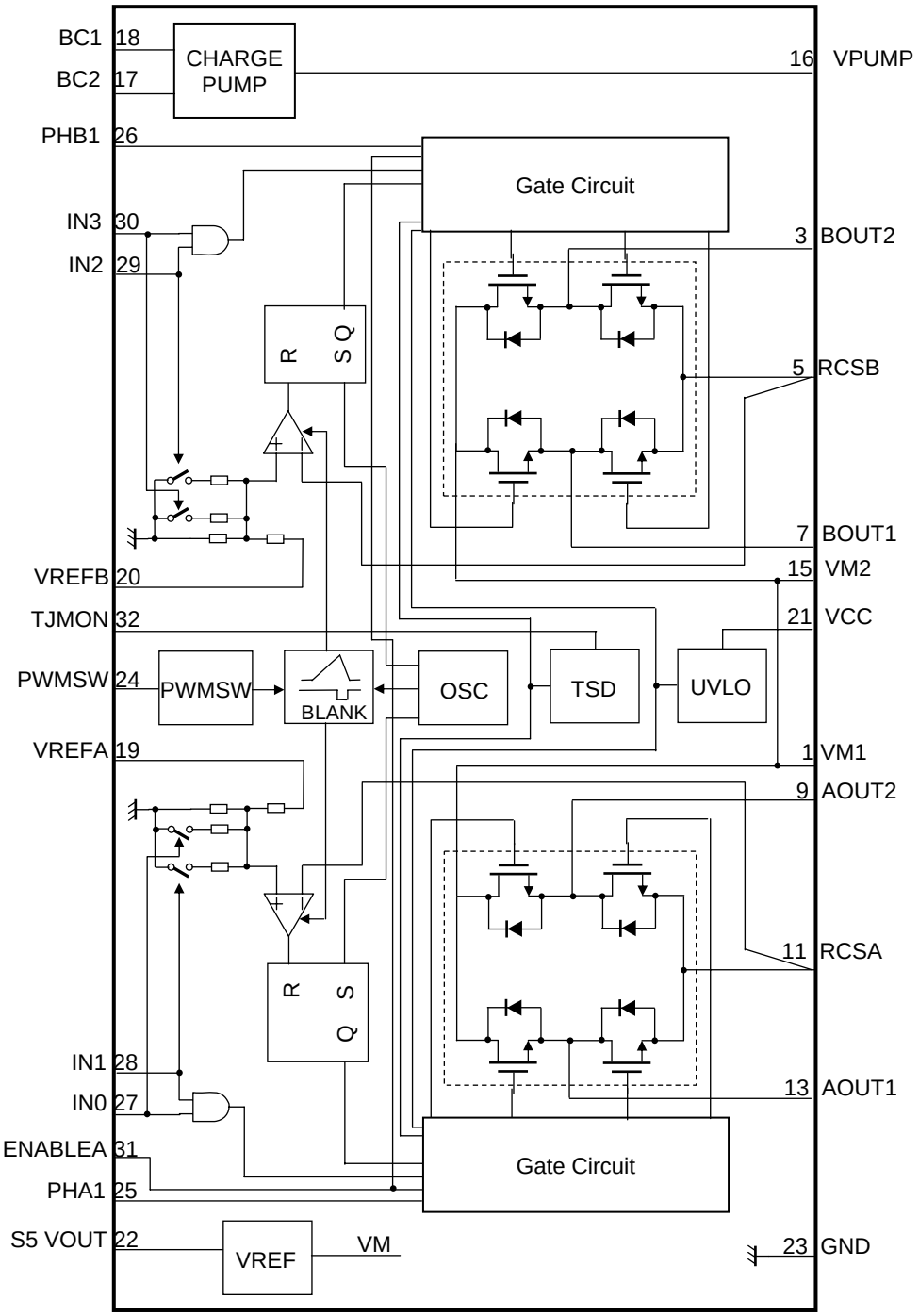


PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	VM1	Power supply	Motor power supply 1
2,4,6,8, 10,12,14	N.C.	—	No Connection
3	BOUT2	Output	Phase B motor drive output 2
5	RCSB	Input / Output	Phase B current detection
7	BOUT1	Output	Phase B motor drive output 1
9	AOUT2	Output	Phase A motor drive output 2
11	RCSA	Input / Output	Phase A current detection
13	AOUT1	Output	Phase A motor drive output 1
15	VM2	Power supply	Motor power supply 2
16	VPUMP	Output	Charge Pump circuit output
17	BC2	Output	Charge Pump capacitor connection 2
18	BC1	Output	Charge Pump capacitor connection 1
19	VREFA	Input	Phase A torque reference voltage input
20	VREFB	Input	Phase B torque reference voltage input
21	VCC	Power supply	Signal power supply
22	S5VOUT	Output	Internal reference voltage (5V output)
23	GND	Ground	Signal ground
24	PWMSW	Input	PWM frequency selection input
25	PHA1	Input	Phase A phase selection input
26	PHB1	Input	Phase B phase selection input
27	IN0	Input	Phase A output torque control 1
28	IN1	Input	Phase A output torque control 2
29	IN2	Input	Phase B output torque control 1
30	IN3	Input	Phase B output torque control 2
31	ENABLEA	Input	Phase A/B Enable/Disable CTL
32	TJMON	Output	VBE monitor use

Notes) Concerning detail about pin description, please refer to OPERATION and APPLICATION INFORMATION section.

FUNCTIONAL BLOCK DIAGRAM



Note) This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

OPERATION

1. Control mode

1) Truth table

ENABLEA	PHA1/PHB1	AOUT1/BOUT1	AOUT2/BOUT2
"L"	"H"	"H"	"L"
"L"	"L"	"L"	"H"
"H"	—	OFF	OFF

IN0/IN2	IN1/IN3	Output Current
"L"	"L"	(VREF / 10) × (1 / Rs) = I_{OUT}
"H"	"L"	(VREF / 10) × (1 / Rs) × (2 / 3) = I_{OUT}
"L"	"H"	(VREF / 10) × (1 / Rs) × (1 / 3) = I_{OUT}
"H"	"H"	0

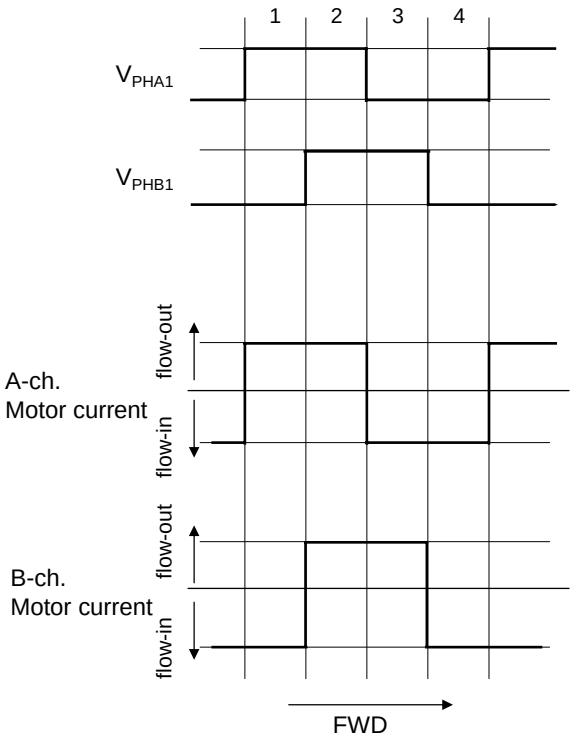
Note1) Rs : current detection region

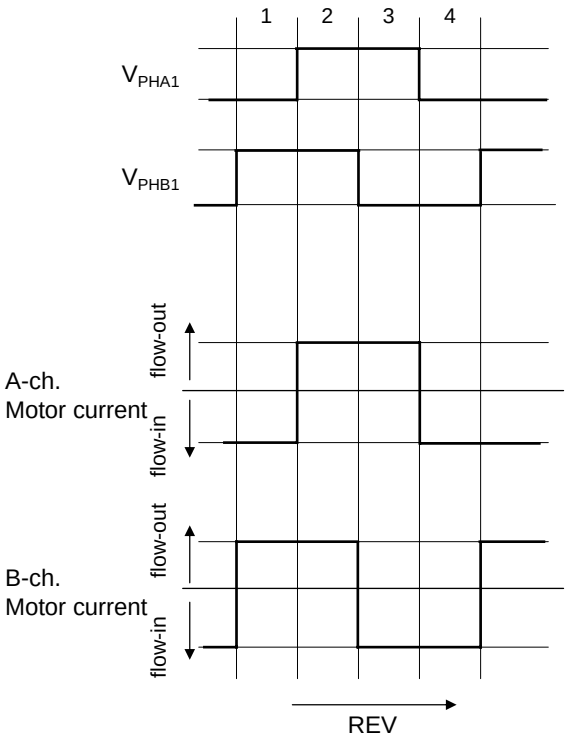
Note2) When ENABLEA = "H" or IN0 = IN1 = "H"/IN2 = IN3 = "H", all output transistors switch off at the same time.

OPERATION (continued)

1. Control mode (continued)

2) Drive of full step (4steps sequence)
(IN0 to IN3 = const.)

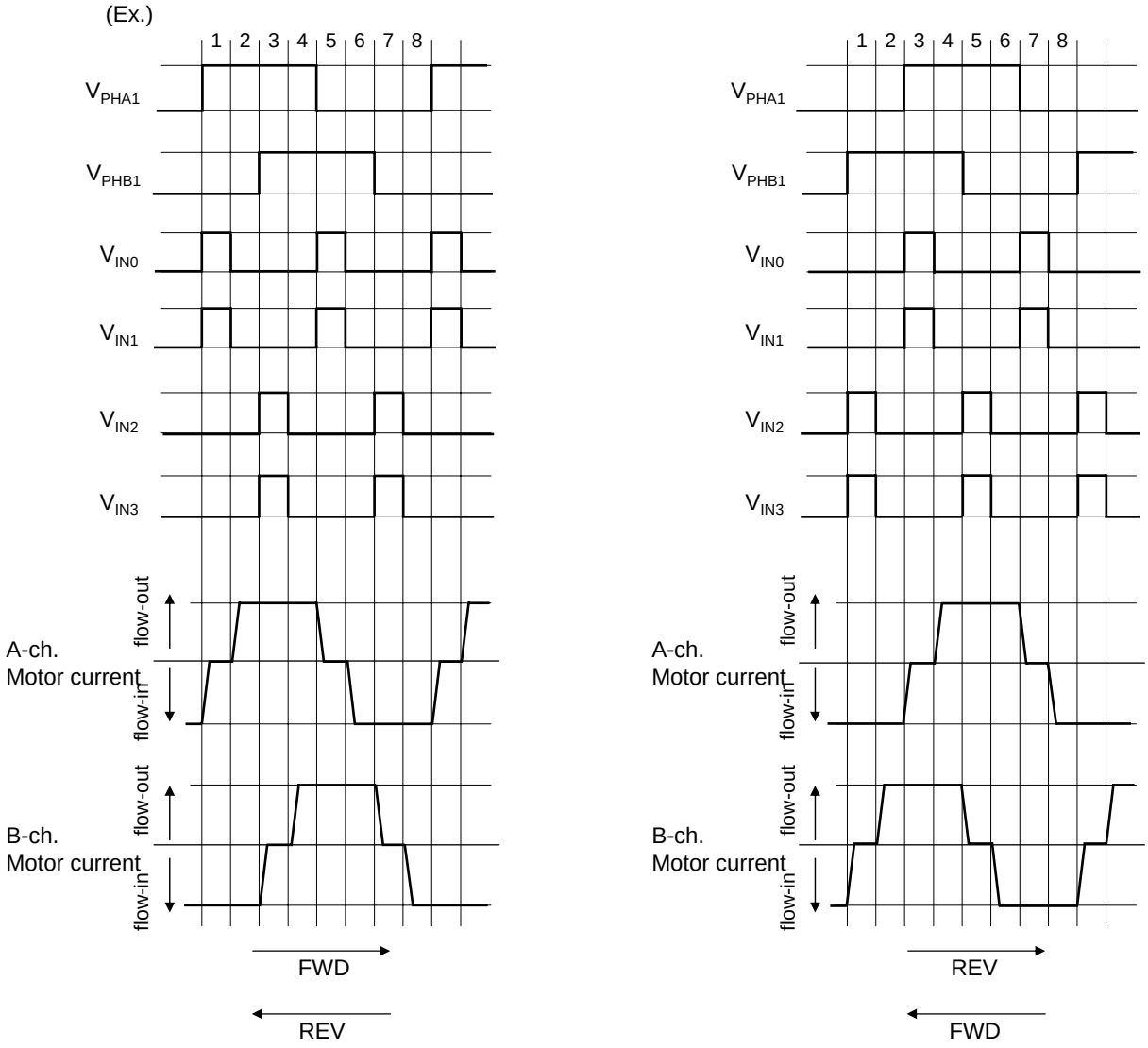




OPERATION (continued)

1. Control mode(continued)

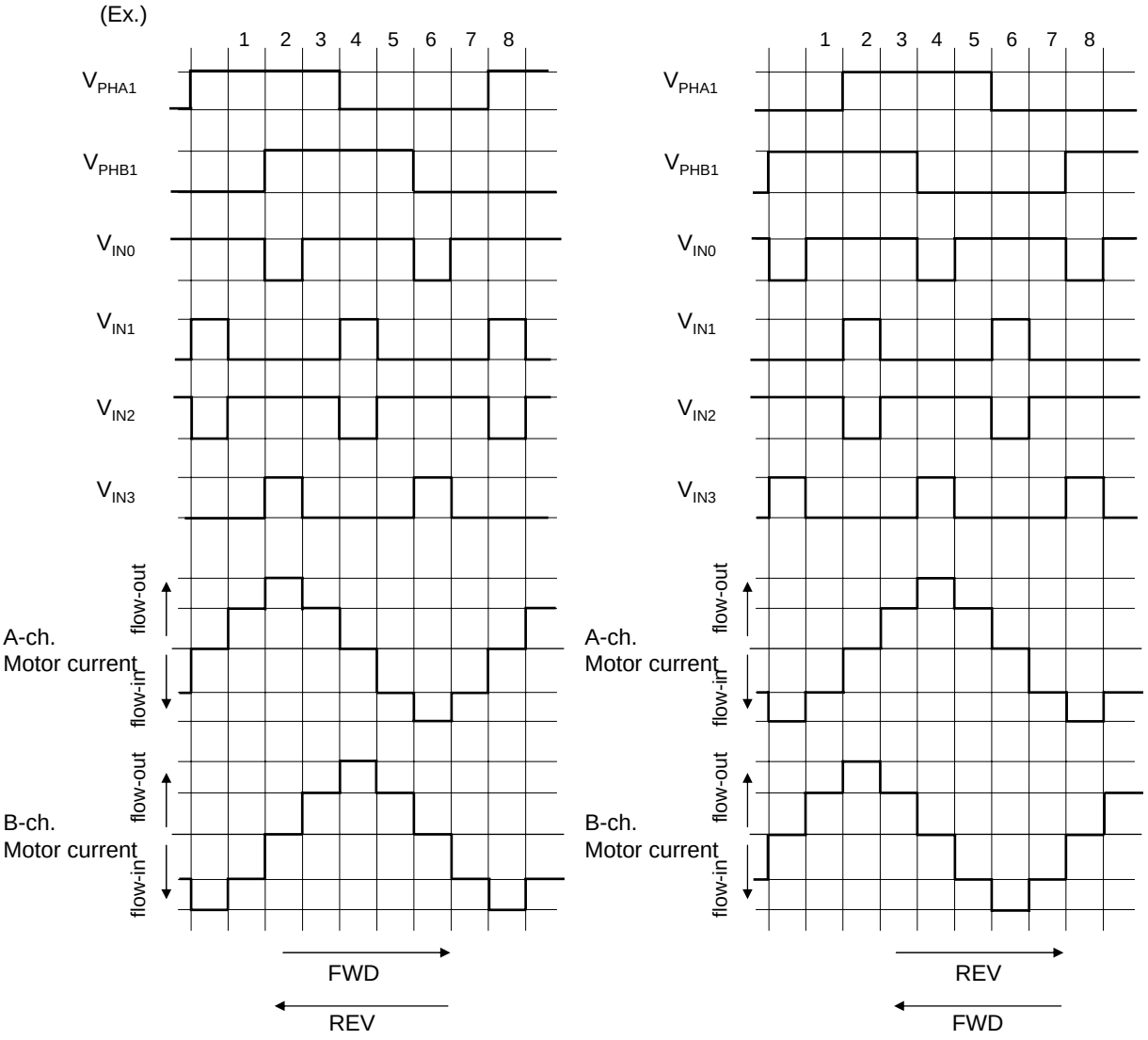
3) Drive of half step (8steps sequence)



OPERATION (continued)

1. Control mode(continued)

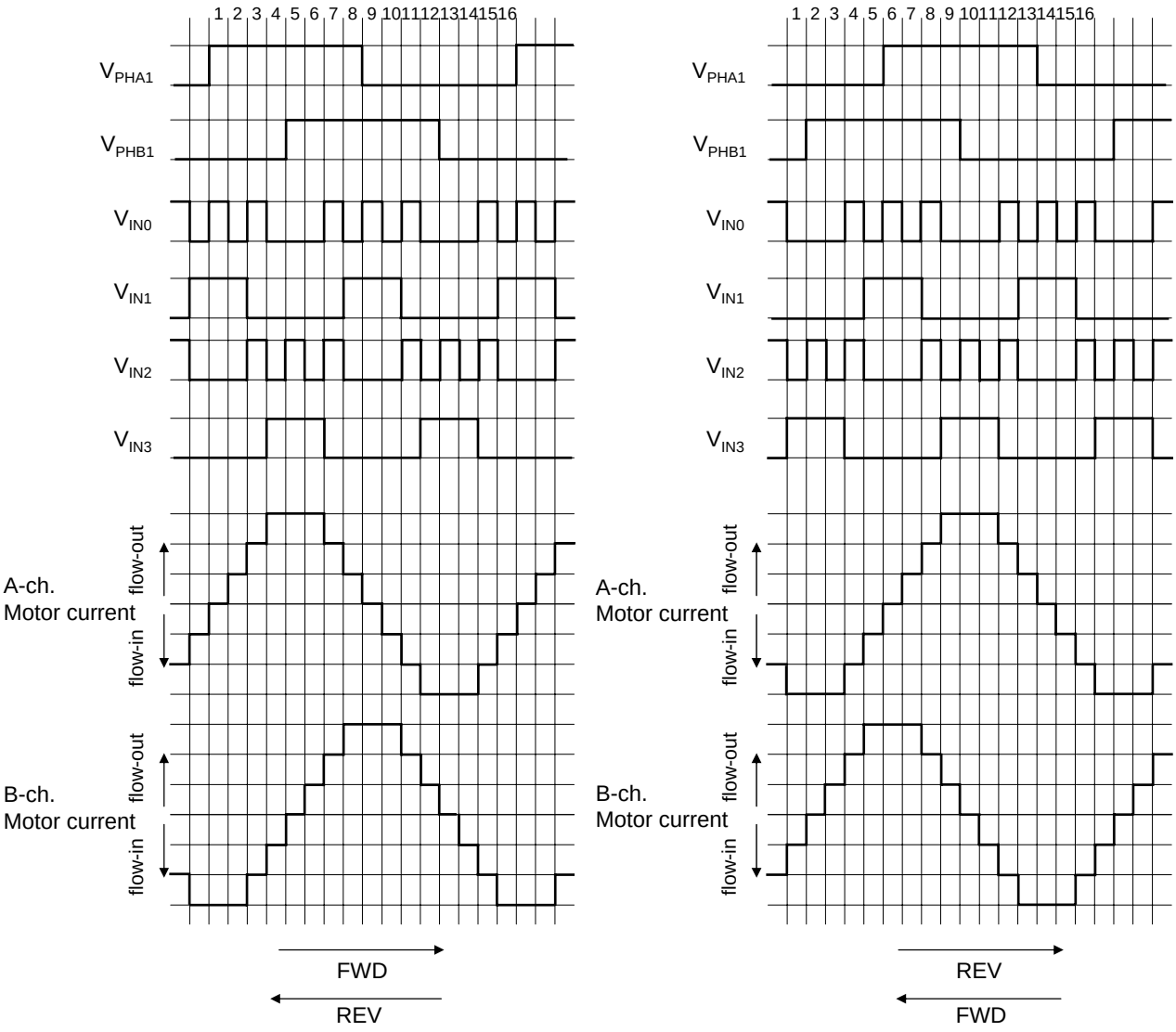
4) 1-2 phase excitation (8steps sequence)



OPERATION (continued)

1. Control mode(continued)

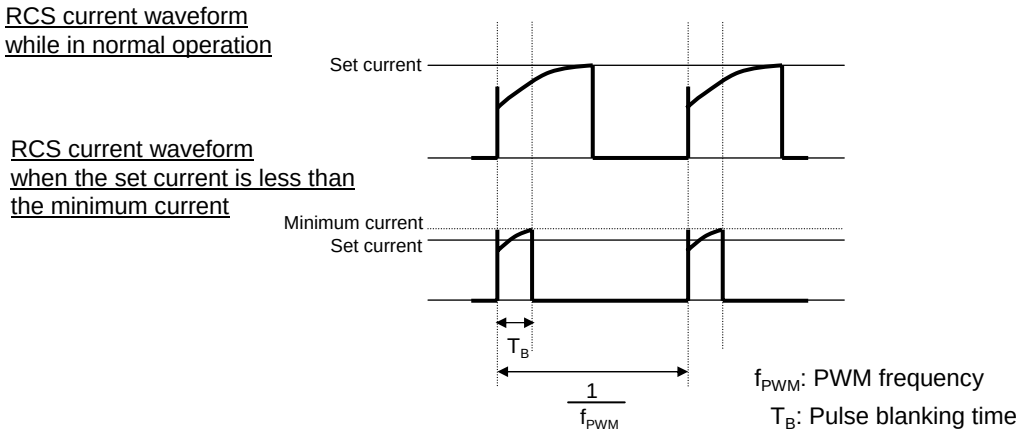
5) W1-2 phase excitation (16steps sequence)



APPLICATIONS INFORMATION

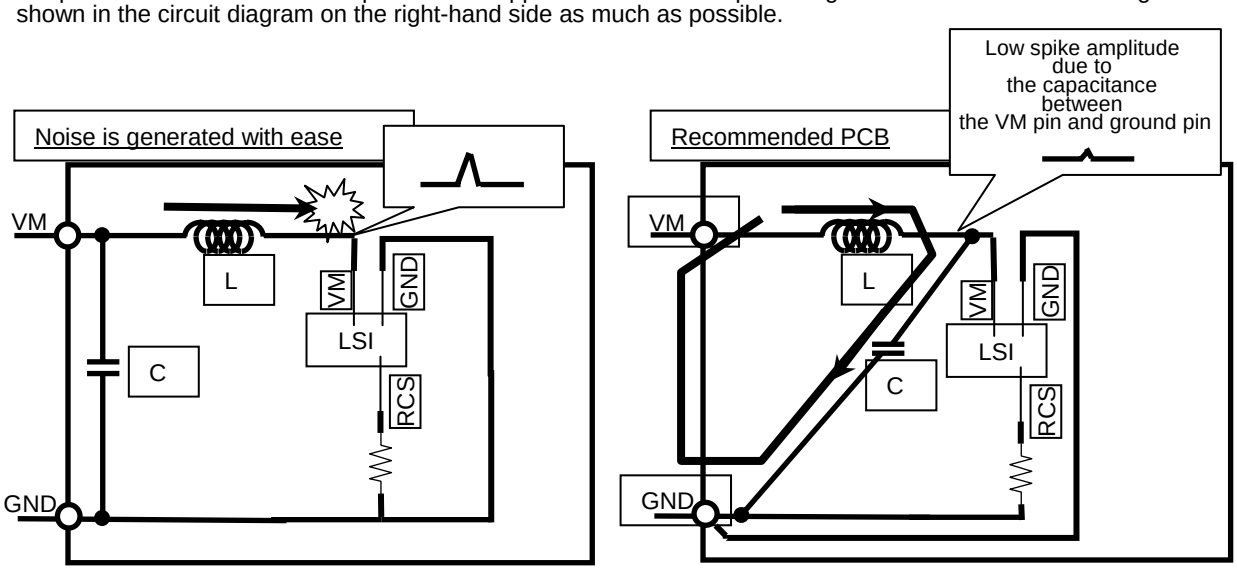
1. Usage Notes

1) In order to prevent mistakes in current detection resulting noise, this LSI is provided with a pulse blanking time of 0.75 µs (typ.).
The motor current will not be less than the current determined by blanking time. Pay utmost attention at the time of minute current control.
The graph on the right-hand side shows the relationship between the pulse blanking time and minute current value.
The increase or decrease in the motor current is determined by the resistance of the internal winding of the motor.



2) A high current flows into the LSI. Therefore, the common impedance of the PCB pattern cannot be ignored. Take the following points into consideration and design the PCB pattern of the motor.

A high current flows into the line between the VM1 (Pin 1) and VM2 (Pin 15) pins. Therefore, noise is generated with ease at the time of switching due to the inductance (L) of the line, which may result in the malfunctioning or destruction of the LSI (see the circuit diagram on the left-hand side). As shown in the circuit diagram on the right-hand side, the escape way of the noise is secured by connecting a capacitor to the connector close to the VM pin of the LSI. This makes it possible to suppress the direct VM pin voltage of the LSI. Make the settings as shown in the circuit diagram on the right-hand side as much as possible.

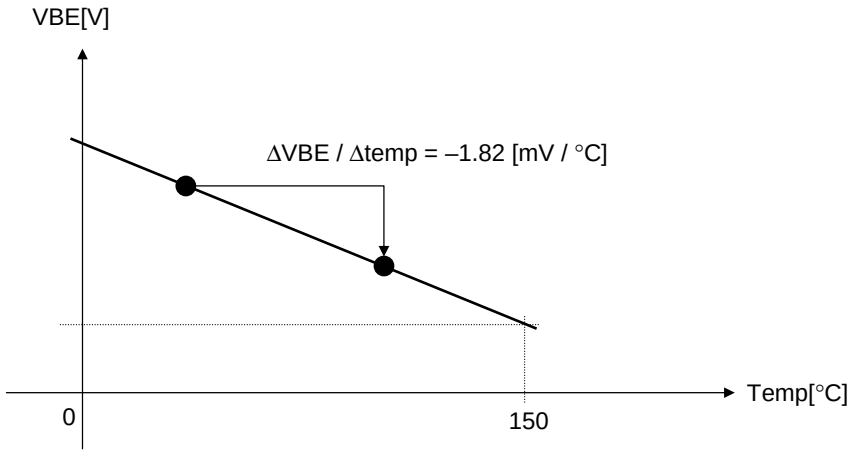


APPLICATIONS INFORMATION (continued)

1. Usage Notes (continued)

3) In the case of measuring the chip temperature of the LSI,measure the voltage of TJMON (Pin 32) and presume chip temperature from following data. Use the following data as reference data. Before applying the LSI to a product, conduct a sufficient reliability test of the LSI along with the evaluation of the product with the LSI incorporated.

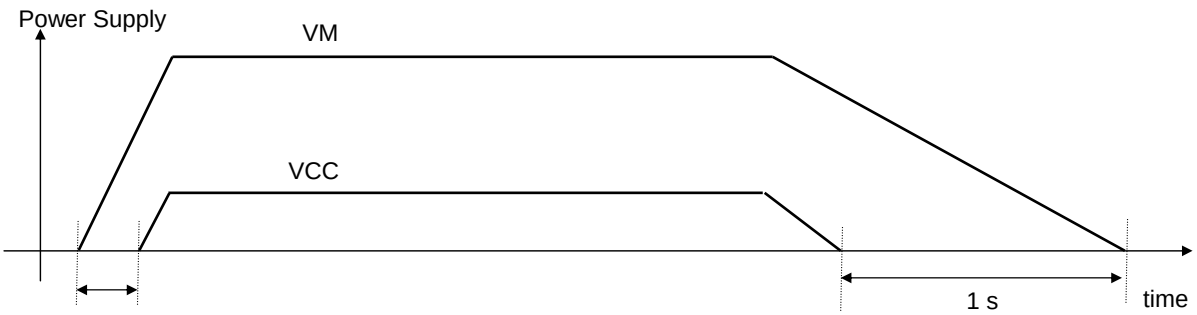
The temperature characteristic of TJMON



4) Power Supply Sequence
If two types of power supply are used
Rise : This LSI is recommended rise of 5 V power supply before rise of 24 V power supply.
Fall : Although there is no particular rule, check that VM fall time is about 1sec.

When recommended sequence is difficult, take the diagram below indicates into consideration and design.

Also, rise slew rate design
VM : below 0.1 V/µs, VCC : below 0.1 V/µs



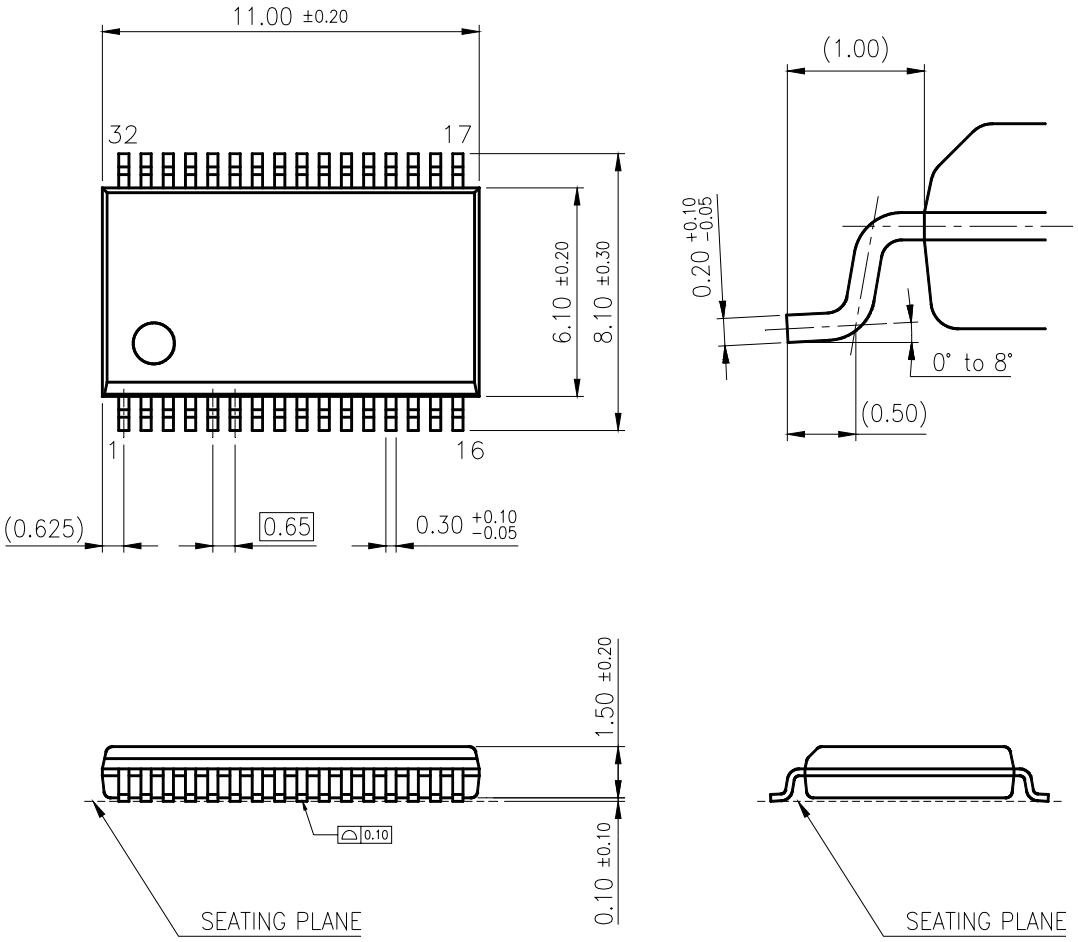
Delay : below 100 ms

If one type of power supply is used
Rise slew rate design
VM : below 0.1 V/µs

5) Check the risk that is caused by the failure of external components.

PACKAGE INFORMATION (Reference Data)

Package Code:SSOP032-P-0300B unit:mm



Body Material	:	Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	SnBi Plating

IMPORTANT NOTICE

1.The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

2.When using the LSI for new models, verify the safety including the long-term reliability for each product.

3.When the application system is designed by using this LSI, be sure to confirm notes in this book.
Be sure to read the notes to descriptions and the usage notes in the book.

4.The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information de-scribed in this book.

5.This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.

6.This LSI is intended to be used for general electronic equipment.
Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
Any applications other than the standard applications intended.
(1) Space appliance (such as artificial satellite, and rocket)
(2) Traffic control equipment (such as for automobile, airplane, train, and ship)
(3) Medical equipment for life support
(4) Submarine transponder
(5) Control equipment for power plant
(6) Disaster prevention and security device
(7) Weapon
(8) Others : Applications of which reliability equivalent to (1) to (7) is required
It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the LSI described in this book for any special application, unless our company agrees to your using the LSI in this book for any special application.

7.This LSI is neither designed nor intended for use in automotive applications or environments unless the specific product is designated by our company as compliant with the ISO/TS 16949 requirements.
Our company shall not be held responsible for any damage incurred by you or any third party as a result of or in connection with your using the LSI in automotive application, unless our company agrees to your using the LSI in this book for such application.

8.If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

9. Please use this product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of your using the LSI not complying with the applicable laws and regulations.

USAGE NOTES

1. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

2. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

3. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

4. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

5. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

6. The LSI is destructed under an abnormal condition, such as the short-circuiting between the output and VM pins, output and ground pins, or output pins (i.e., load short-circuiting), in which case smoke may be generated. Pay utmost attention to the use of the LSI.

   Pay special attention to the following pins so that they are not short-circuited with the VM pin, ground pin, other output pin, or current detection pin.
   (1) AOUT1 (Pin 13), AOUT2 (Pin 9), BOUT1 (Pin 7), BOUT2 (Pin 3)
   (2) BC2 (Pin 17), VPUMP (Pin 16)
   (3) VM1 (Pin 1), VM2 (Pin 15), VCC(Pin 21), S5 VOUT(Pin 22)
   (4) RCSA (Pin 11), RCSB (Pin 5)

   The higher the current capacity of power supply is, the higher the possibility of the above destruction or smoke generation. Therefore, it is recommended to take safety countermeasures, such as the use of a fuse.

7. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VM short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.

8. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

9. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.

10. Verify the risks which might be caused by the malfunctions of external components.

USAGE NOTES (continued)

11. Perform thermal design work with consideration of a sufficient margin to keep the power dissipation based on supply voltage, load, and ambient temperature conditions.
(The LSI is recommended that junctions are designed below 70% to 80% of Absolute Maximum Rating.)

12. Set the value of the capacitor between the VPUMP and GND pins so that the voltage on the VPUMP (Pin 16) will not exceed 43 V in any case regardless of whether it is a transient phenomenon or not while the motor standing by is started.

13. This LSI employs a PWM drive method that switches the high-current output of the output transistor. Therefore, the LSI is apt to generate noise that may cause the LSI to malfunction or have fatal damage. To prevent these problems, the power supply must be stable enough. Therefore, the capacitance between the VCC and GND pins must be a minimum of 0.1 μF and the one between the VM and GND pins must be a minimum of 47 μF and as close as possible to the LSI so that PWM noise will not cause the LSI to malfunction or have fatal damage.

Request for your special attention and precautions in using the technical information and semiconductors described in this book

(1) If any of the products or technical information described in this book is to be exported or provided to non-residents, the laws and regulations of the exporting country, especially, those with regard to security export control, must be observed.

(2) The technical information described in this book is intended only to show the main characteristics and application circuit examples of the products. No license is granted in and to any intellectual property right or other right owned by Panasonic Corporation or any other company. Therefore, no responsibility is assumed by our company as to the infringement upon any such right owned by any other company which may arise as a result of the use of technical information described in this book.

(3) The products described in this book are intended to be used for general applications (such as office equipment, communications equipment, measuring instruments and household appliances), or for specific applications as expressly stated in this book.
Consult our sales staff in advance for information on the following applications:
- Special applications (such as for airplanes, aerospace, automotive equipment, traffic signaling equipment, combustion equipment, life support systems and safety devices) in which exceptional quality and reliability are required, or if the failure or malfunction of the products may directly jeopardize life or harm the human body.

It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the products described in this book for any special application, unless our company agrees to your using the products in this book for any special application.

(4) The products and product specifications described in this book are subject to change without notice for modification and/or improvement. At the final stage of your design, purchasing, or use of the products, therefore, ask for the most up-to-date Product Standards in advance to make sure that the latest specifications satisfy your requirements.

(5) When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(6) Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process. When using products for which damp-proof packing is required, satisfy the conditions, such as shelf life and the elapsed time since first opening the packages.

(7) This book may be not reprinted or reproduced whether wholly or partially, without the prior written permission of our company.

20100202